Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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Understanding and using high-speed clamp amplifiers (page 13)
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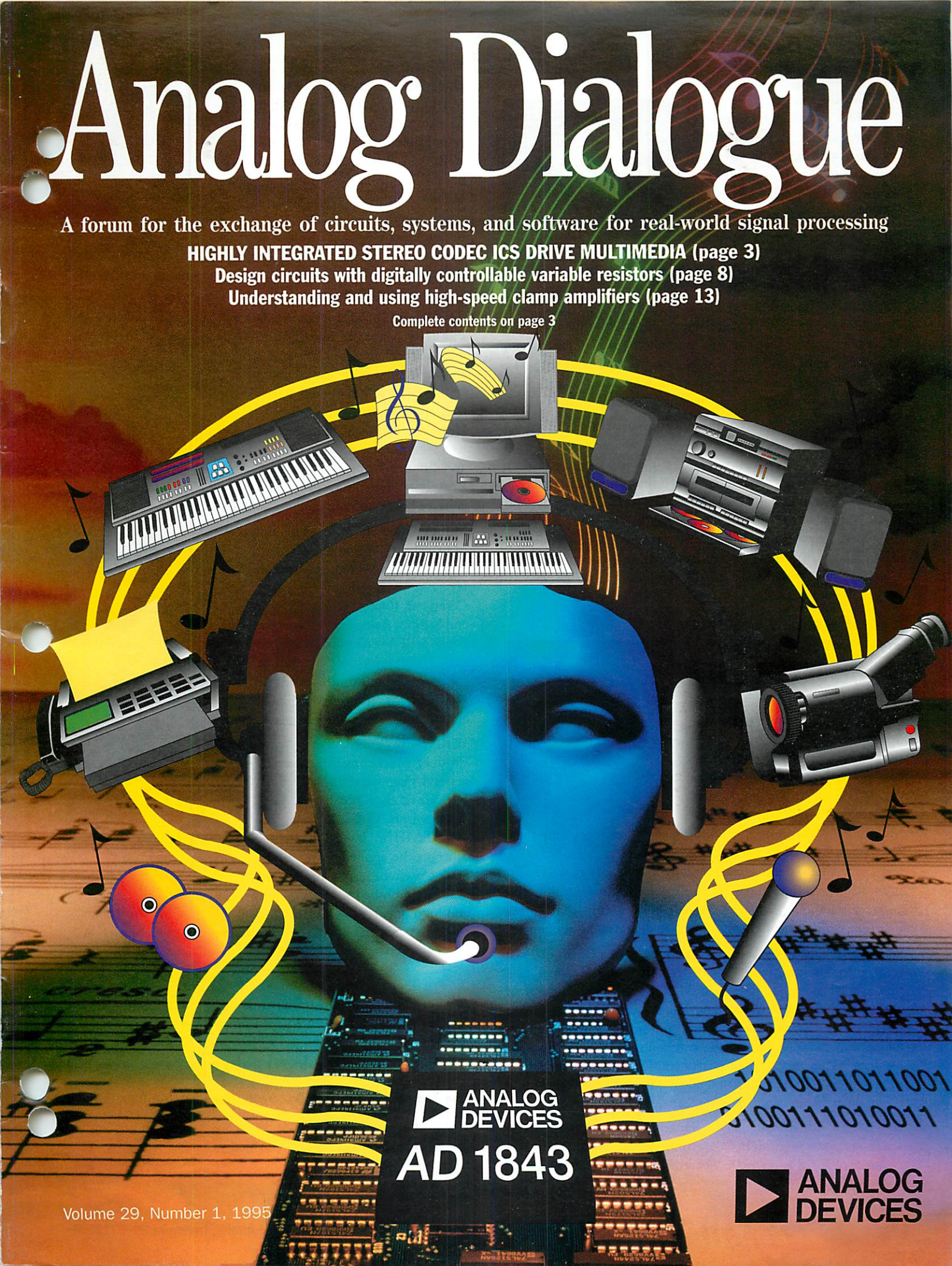


Volume 29, Number 1, 1995

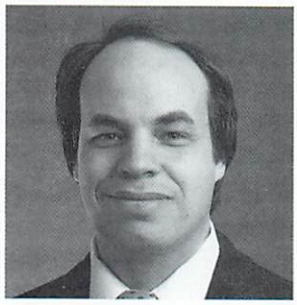
Editor's Notes

KEEPING UP

How does a staff of hundreds of technologists in an international company with far-flung activities keep abreast of technical ideas and information being generated within their company? Fax, phone, newsletters, and computer communication networks, such as the Internet, are easy answers. But beyond that, how does a junior engineer from half a world away get to have an unanticipated chat with the likes of Barrie Gilbert, Paul Brokaw, or Jody Lapham? How does a Ray Stata or Jerry Fishman get vital feedback from informal personal contact with designers, semiconductor process people, software experts, applications engineers? How do problems waiting to be solved and solutions waiting to be applied meet serendipitously?

At Analog Devices, things like this happen every year at our annual General Technical Conference, when engineers and scientists from all over the world converge on a hotel site in Massachusetts. They give and listen to papers, join in workshops, drink beer and break bread together, and shoot the breeze in hallways, for two days and more. Many of them receive patent awards and, in most years, one or two very lucky (and deserving) technologists are named to the Pantheon of Fellows, the highest step on our parallel career ladder. Who benefits? We all do, including especially—and ultimately—our customers.

BOB ADAMS RECEIVES AES SILVER MEDAL



Robert W. Adams, a Fellow of the Audio Engineering Society (*Analog Dialogue* 25-2), has been awarded the Society's Silver Medal "for outstanding contributions to the advancement of digital audio technology." Bob is best known in the industry for his significant influence on the theory and practical realization of high-precision oversampling A/D and D/A converters and their measurement—and for the design of such devices as the AD1879, an 18-bit sigma-delta converter for stereo. His more-recent innovations include the AD1890 asynchronous sample-rate converter (*Analog Dialogue* 28-1, 1994), a chip that solves interfacing and compatibility problems in digital audio equipment.

Adams was born in Syracuse, NY and received a BSEE in 1976 from Tufts University, Medford MA. After a brief career as a professional musician, he joined ADS, Inc., a manufacturer of automotive audio electronics and loudspeakers. From 1977, at dbx, inc., he designed oversampling converters for digital audio, and later became Director of Research. Products resulting from his work include a recording system employing companded delta modulation—and later, a 20-bit standalone A/D converter using sigma-delta technology. He joined Analog Devices in 1989.

Bob has published many papers under the auspices of AES and IEEE and has been awarded several circuit patents. He is a Member of IEEE and a Fellow of AES.

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Al Haun (p. 3), Technical-Publicity Manager for ADI, Al manages technical press relations and trade show programs. Joining ADI in 1970, he has worked in test, QC, applications, and marketing. He holds a certificate in electronics technology and a BS in marketing and finance from Northeastern University. His interests include golf, ice hockey, stocks, and building colonial-style furniture.

Maury Wood (p. 3), is Marketing Manager, IC Sound Products, in ADI's Computer Products Division. He has worked at Mercury Computer, Cypress Semiconductor, and Sanders Associates. Maury has BSEE & BFA in Music degrees from the University of Michigan, followed by graduate study at Northeastern. In his spare time he enjoys mountain biking and telemark skiing.

Walt Heinzer (p. 8), is New-Product Marketing Manager for general-purpose data-conversion ICs. He received BSEE and MSEE degrees from U. C., Berkeley and joined ADI in 1982. Earlier, at Siliconix, he applied power FETs, analog switches, and converters. Walt has published technical papers and contributed to the McGraw-Hill book, *Designing with Field-Effect Transistors.* He enjoys hiking and photography.

[more authors on page 22]

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Highly Integrated Stereo Codec ICs Drive Multimedia

AD1843 combines fax/modem and games compatible audio capabilities, includes sample-rate conversion. AD1845 exceeds MPC Level-2 requirements

by Dave Babicz, Maury Wood and Al Haun

However we define "multimedia", one thing is certain: add-in card manufacturers have had great success in marketing sound cards and kits to upgrade PCs for multimedia. These kits usually include a CD-ROM drive, a sound card, bundled software, and external powered speakers. Though games are a classical add-on capability, even more popular are *modem* functions—and more recently, *fax*/modems. This demand has been driven by the explosion in the use of on-line services, plus the many practical and business-oriented uses for both modems and faxes.

Now low-cost highly integrated codecs allow PC manufacturers to offer combinations of audio, fax, and modem capability on a single add-in card, or even on the motherboard. The basic function of a codec (*co*der/*dec*oder) involves A/D conversion to produce digital code from analog signals and D/A conversion to convert processed code back to analog. But modern codecs can do far more—and on a single chip. Two examples of these analog "front ends" will be discussed here: the new—and very versatile—AD1843* SoundComm™ codec, which can process a variety of concurrent signals having differing sample rates, and the AD1845* SoundPort® stereo codec, which includes programmable sample rates, advanced power management features, and backward-compatibility with existing industry-standard codecs.

DSP IS THE KEY

Sound card makers are quickly and increasingly moving to software-programmable DSP-based solutions and away from fixed-function circuitry; *flexibility* is the reason. There are simply too many optional signal-processing tasks for dedicated fixed-function hardware to handle with reasonable use of space, cost, and power. When this digital adroitness is interfaced using flexible codecs—which offer many modes of combining and processing analog inputs on-chip—powerful systems can be built with little additional hardware (Figure 1). Such systems make available a host of signal-generation synthesis and processing options for cost-effective integration of sound-processing and communications functions.

For example, synthesis alternatives include frequency modulation, wavetable lookup, and physical instrument modeling; and signal processing alternatives include equalization, control of dynamics, and spatial effects.

With a programmable processor, changing the synthesis method or the signal-manipulation process is a simple matter of downloading a new algorithm set. Similarly, the multitude of standards for data modems (including V.34, V.32ter and V.32bis) and fax modems (including V.17, V.27ter and V.29) calls for a programmable DSP strategy. A library of algorithms makes possible a software-based, or "soft-modem", design implementation—where the required routine is downloaded and invoked when needed. Accordingly, many modem products have been announced with DSP chip data pumps/controllers. Since DSP engines are the key to sound and fax/modem functions, a single DSP can support both, saving cost and space.

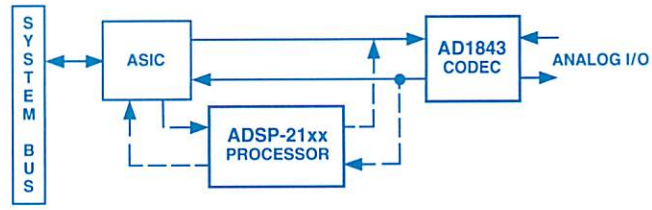

Figure 1. Typical system diagram using the AD1843, an ADSP-21xx series DSP and a bus interface ASIC to provide a high performance PC-based audio/telephony system.

Another factor driving the integration of audio with fax/modems is the similar nature of their signal processing requirements. Both sound record/playback and full duplex public-service telephone-network (PSTN)-oriented data communications require an analog front-end, generally consisting of analog-to-digital and digital-to-analog converters and associated analog processing circuitry. The signal-quality requirements to support advanced data-modem standards, such as V.34, are essentially identical to those needed for "business audio" and games-compatible audio. A combined audio/fax/modem analog front-end, with enough signal conversion capability, clocking, and communication bandwidth, could allow these functions to live together concurrently. As evidence that this is becoming the industry direction, a standard now under discussion, MPC3 (multimedia 3), includes audio record/ playback and fax/modem capabilities.

EXAMPLES OF CONCURRENT APPLICATIONS

Stereo codecs have paired ADC and DAC functions. In the AD1843, when used to their fullest capacity, they can support a wide range of applications. The possibilities include:

- Full-duplex V.34 (or fallbacks) data modem (including phase- and frequency re-sampling for PSTN echo-cancellation) *and* simultaneous CD-quality stereo audio playback
- Stereo audio capture, four-channel audio playback with high-quality audio/video synchronization for H.320 video teleconferencing or MPEG-based systems.

*Use the reply card for technical data. Circle 1

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- Full duplex acoustic echo-canceling speakerphone with stereo audio playback for business applications
- Digital simultaneous voice-over-data for consumer telegaming applications.

AD1843 SoundComm™ Multimedia Codec Handles Speech, Audio, Fax/Modem Signals

The AD1843 is a complete input/output analog interface for high-performance DSP-based telephony and audio applications. Integrated on this single chip are circuits needed to fulfill the real-world analog I/O requirements for many popular functions, thus reducing system size, power consumption, and complexity.

The main elements of the AD1843 (Figure 2) are: an extensive input and mixing section; two channels of sigma-delta (Σ-Δ) analog-to-digital conversion; four channels of Σ-Δ digital-to-analog conversion; digital filters; and control circuitry for implementing the device's different modes of operation. The AD1843 permits flexible sample-rate selection through programming and synchronization to external clocks, many input and output options, and many mixing options.

Here are some examples of functions it can perform:

- stereophonic audio input and/or quad output, simultaneously
- stereo audio output with simultaneous modem or fax functions
- monophonic audio input and output with simultaneous modem receive and transmit for simultaneous voice and data communications
- dual independent audio input with audio output for echo-canceling speaker-phones

Audio functions and performance

The AD1843's dynamic range exceeds 80 dB over the 20-kHz audio band, and it supports sample rates from 4 kHz to 54 kHz. Its audio functions are based on, but considerably exceed in variety, those found in the Analog Devices AD1848 SoundPort® codec. The AD1848 has set the business-audio standard throughout the computer industry (*Analog Dialogue* 27-1, 1993, pp. 7-8).

Inputs to the device include: a stereo microphone pair; a stereo line pair; a stereo CD input pair (AUX1); a stereo synthesized music input pair (AUX2); a dual phone-line input (AUX3); a monophonic input; and a stereo input from an FM synthesizer (SUM). All of these inputs (except SUM) are multiplexed to the A/D converter pair and can be mixed directly as analog signals with the outputs of the D/A converters. All analog input signals (except SUM) can be subjected to gain, attenuation or muting (GAM blocks) before they are mixed with the outputs of the D/A converters.

The device's two pairs of DACs accept 16-bit digital data from the serial port. Each DAC pair has an independent sampling rate, which can either be programmed by a control register or synchronized to an external clock. The second pair of DACs can

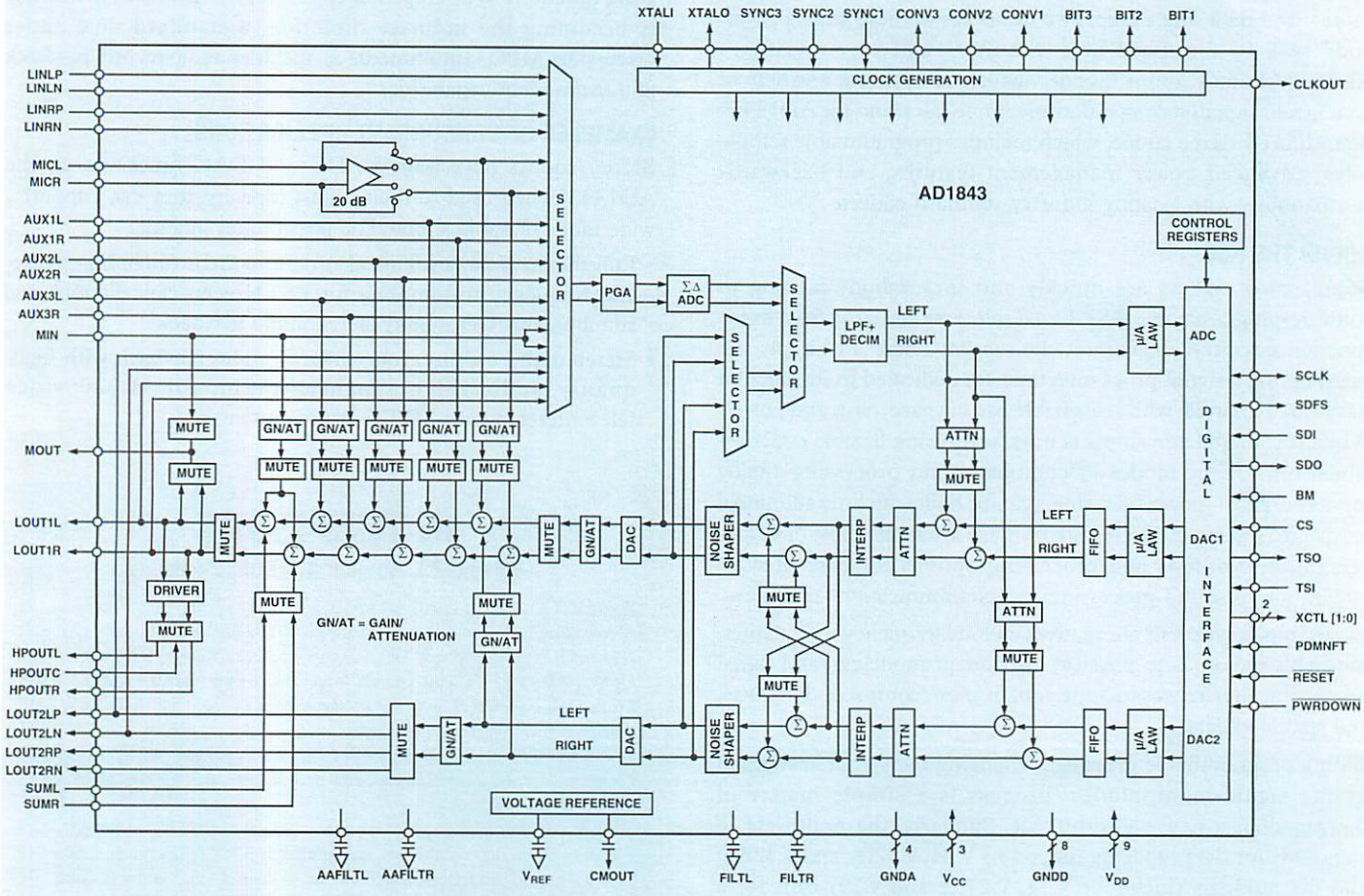


Figure 2. AD1843 functional block diagram.

be used to fill the function of the music-synthesis DAC pair found on many audio products offered for PCs. Analog outputs from the AD1843 include a line output, a monophonic output, a three-wire stereo headphone output with its own return path, and a differential stereo output for connection to a DAA (direct access arrangement—a PSTN interface). The line and differential outputs are looped back to the ADC input selector for monitoring, further processing, etc.

The AD1843's analog and digital mixing and routing capabilities are extensive. The digital data from both DAC channels—after interpolation, but prior to noise shaping—can be routed back to the ADC decimators to support digital-to-digital sample rate conversion. Digital data from the ADCs can be routed to the two stereo DAC pairs for a digital loopback mode—helpful for device-level and board-level test. Digital data from either stereo DAC pair can be mixed with the digital data feeding the other DAC pair, and the analog output signals from the DAC pairs can also be mixed.

On-Chip Sample-Rate Conversion:

The AD1843 operates from a single external clock or crystal source, from which a wide range of sample rates can be generated. When the AD1843 is driven from a 24.576-MHz input frequency source, its three phase-locked-loop sample clock generators can be individually programmed to generate any sample frequency from 4 kHz to 54 kHz with 1-Hz resolution. The sample clocks can be individually synchronized, either to the device's input frequency source or to external clocks, and all sample rate changes can be made dynamically, i.e., "on the fly". Each A/D converter and the two D/A stereo converter pairs can individually be sampled at any of the three sample-clock rates, or at a fixed 48.0 kHz.

SYNC Audio to Video

SYNC inputs can also be used in a special mode for audio/video synchronization. In this mode, when an NTSC- or PAL-compatible horizontal sync signal (approximately 15 kHz) is applied to the SYNC inputs, the device produces one of four standard audio sample rates (32, 44.056, 44.1, and 48 kHz). In this manner, video and audio sample rates, though not rationally related, can be "locked" together.

PSTN Communications Functional Description

The AD1843 includes all data conversion, filtering, and clock generation circuitry needed to implement an echo-canceling modem with a single companion DSP. Three bit clocks with software-programmable sample rates and clocking modes support all established modem standards—plus those for the V.34 standard.

The AD1843's advanced oversampling technology moves the entire echo-canceling modem implementation into the digital domain. The device maintains 85-dB SNR and THD throughout all filtering and data conversion. Wholly DSP-based echo cancellation algorithms can maintain robust bit error rates despite worst-case signal attenuation and echo amplitudes. The AD1843's on-chip interpolation filter re-samples the received signal after echo cancellation in the DSP, freeing the processor for other voice or data communications tasks.

On-chip bit- and baud clock generation circuitry allows either synchronous or asynchronous operation of the transmit (DAC) and receive (ADC) paths. Each path features independent phase-advance and -retard adjustments under software control. The AD1843 can also synchronize modem operation to an externally connected bit clock.

With its multiple input and output channels and converters, the AD1843 is well suited for telephony applications requiring multiple channels for voice and modem.

Many options for conserving power

With the proliferation of portable computing/communications products and the "greening" of the PC, advanced power management techniques have become an urgent necessity. Recognizing this, the AD1843 goes well beyond conventional battery-saving whole-chip power-down. Control bits allow the user to selectively power down unused sections of the chip, including: the ADC channels (left and right, separately); DAC1 and DAC2; the stereo headphone driver; and the analog mixer.

It is also possible to power down the analog portions of the DACs, when analog-in/analog-out mixing and digital-in/digital-out re-sampling are the only needed functions. Furthermore, individual power-down control is provided for the three clock generators, as well as for the three bit-clock outputs and the three conversion-clock outputs. And under "global control", a single control bit powers down everything except the serial port, the clock generators, and the crystal oscillator. Finally, a package pin permits external power-down of all on-chip circuitry.

Third-Generation SoundPort® Supports Full-Duplex Asynchronous Operation, Exceeds MPC Level-2 Requirements

The AD1845 16-bit stereo codec integrates all asynchronous audio data conversion and control functions for PC-based audio and multimedia applications. Exemplifying the third generation of 16-bit stereo codecs, the AD1845—the latest member of Analog's SoundPort® family—provides enhancements in performance, integration and power management. With its integral on-chip sample-rate conversion (SRC), a technology previously found only in professional audio gear [see "Asynchronous sample-rate converters", *Analog Dialogue* 28-1 (1994), pp. 8-11], various audio sources with different sample rates can be synchronized.

The AD1845 is also "backward-compatible" with earlier generations of ADI codecs and is pin-compatible with other industry-standard codecs, with the added system benefits provided by on-chip SRC. An on-chip variable sample-frequency generator allows the codec to immediately change sample rates over a range from 4 kHz to 50 kHz, with a resolution of 1 Hz, greatly simplifying the mixing of signals sampled at different rates. In recording or playback, this facility eliminates artifacts in the output, such as unwanted "clicks" and "pops"—common in games applications where audible pitch changes are often generated when the sample rate is changed.

The codec's variable sample-frequency generator is also used to derive all internal clocks from a single user-chosen clock input at 14.31818 MHz, 24 MHz, 24.576 MHz, 25 MHz, or 33 MHz. Other features include: full-duplex operation—which allows

simultaneous record/playback in audio or speak/listen in telephony applications; FIFO (first-in, first-out) buffer to maintain the smooth flow of data, in both capture and playback; power management; and more mixing capability than any audio codec available today.

The AD1845 combines the key audio data-conversion and control functions in a single integrated circuit. The codec includes: stereo audio A/D and D/A converters; complete on-chip filtering; MPC Level-2 compliant analog mixing; programmable gain, attenuation, and muting ("GAM"), and the ability to support advanced power-down modes—plus the variable sample-frequency generator and FIFO. The AD1845 provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card.

Supporting Full Duplex Operation

The AD1845 supports a direct memory-access (DMA) request/grant architecture for transferring data over the host computer bus. It can support either one or two DMA channels. Programmed input/output (PIO) mode is also supported for control-register accesses and for applications lacking DMA control. Two input control lines support mixed "direct" and "indirect" addressing of thirty-seven internal control registers over this asynchronous interface. In addition, the AD1845 includes dual DMA count registers for full-duplex operation; this enables the codec to capture data on one DMA channel and play back data on a separate channel. The 16-sample-deep FIFOs in the capture and playback paths buffer data transfers and reduce the risk of losing data when making DMA transfers via the ISA/EISA bus.

The pair of 16-bit outputs from the ADCs is available over a byte-wide bi-directional interface that also supports 16-bit digital input to the DACs and control information. The AD1845 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The DACs are preceded by a digital interpolation filter. Attenuators provide independent user volume control over the L-and R DAC channels. Nyquist images and shaped quantized noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output. Dynamic range exceeds 80 dB over the 20-kHz audio band.

Only a small number of low cost components are needed for external support. For example, anti-imaging DAC output filters are incorporated on chip, as are built-in 16-mA bus drivers; this eliminates the need for external bus-driver chips in many applications.

Extensive Power Management

The AD1845 provides a variety of hardware- and software low-power and power-down modes to reduce power consumption and extend battery life in notebook and portable computer multimedia applications. For example, the ADC, DAC, and mixer paths can be independently suspended, allowing the AD1845 to be used in capture-only, playback-only, or mixer-only modes.

The analog design team for these codecs was led by Tom Guy, in Wilmington, MA; and the digital design team was led by Analog Devices Fellow, Jim Wilson, based in Norwood, MA.

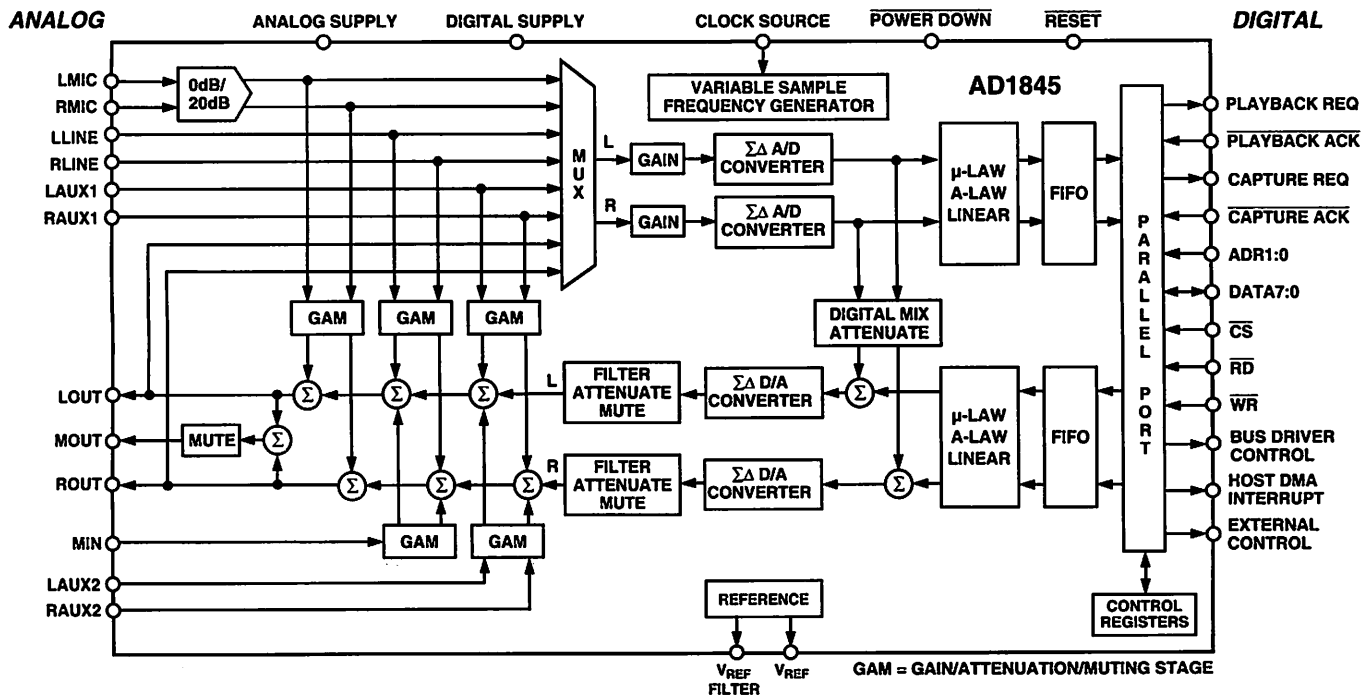


Figure 3. AD1845 functional block diagram ("GAM" = Gain/Attenuation/Muting stage).

Wideband, Low-Cost, Low Power, Single-Supply Current-Feedback Op Amp

AD8011 has 300-MHz bandwidth (G=+1), Draws 1 mA on +5-V supply, Settles to <0.1% in 29 ns

The AD8011* is a very low power (5 mW quiescent), high-speed monolithic op amp specified for operation on +5 or ±5-V supplies. It is a current-feedback (transimpedance) amplifier using a novel two-stage circuit architecture (patent pending) and is fabricated at Analog Devices in a new XFCB (eXtra-Fast Complementary Bipolar) trench-isolation process. The combined process and architecture result in an amplifier that achieves twice the speed on half the power of any amplifier available today. In addition, the proven process, using bonded wafers with deep trenches to achieve full dielectric isolation for high speed at low power, is associated with small die size, hence many dice per wafer, with the resulting benefit of low cost ($1.95 in 1000s).

Salient specifications at +5 V include superior gain flatness (0.1 dB to 20 MHz at a gain of +2—see Figure 1); –3-dB bandwidth of 300 MHz at G = +1 and 180 MHz at G = +2; slew rate of 2000 V/μs; and settling time of 29 ns to 0.1%.

For video applications, its differential gain error is only 0.02%, with differential phase error of 0.06° (single +5-V supply, 1-kΩ load). Distortion is low, with worst harmonics of –70 dBc at 5 MHz and –62 dBc at 20 MHz (Figure 2).

The AD8011 has voltage offset of ±6 mV max over temperature, offset tempco of ±10 μV/°C, and input bias current of ±20 μA max over temperature. Voltage noise is 2 nV/$\sqrt{\text{Hz}}$, and current noise is 5 pA/$\sqrt{\text{Hz}}$. Open-loop transresistance is typically 1.3 MΩ (800 kΩ min). The feedback resistance used is typically 1 kΩ, but it can be reduced for more bandwidth at higher gains

The combination of low power drain, ability to operate with a single supply, and small size (8-pin miniDIP or SOIC package) make it an ideal choice for wideband applications in portable and battery-powered equipment, as well as to replace power-hungry amplifiers having equivalent performance. The AD8011 operates over the extended industrial range (–40°C to +85°C). With a +5-V supply, it is specified for 2.6-V minimum output swing (1.2 to 3.8 V)—compatible with 2.5-V references—with 15 mA minimum output current over temperature. Typical short-circuit current is 50 mA.

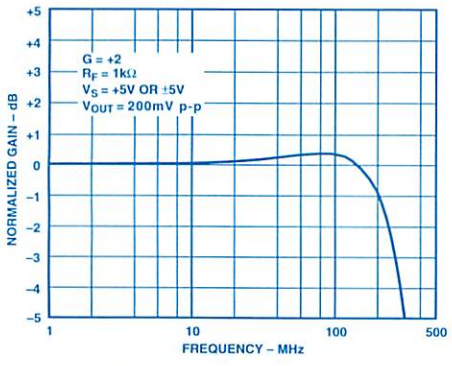


Figure 1. Frequency response, gain of +2.

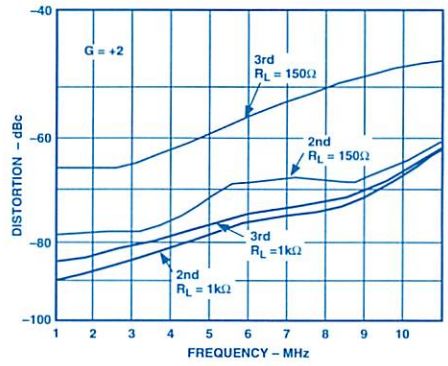


Figure 2. Distortion as a function of frequency, Vs = ±5 V.

APPLICATIONS

Applications for high-performance, low-power, low-cost amplifiers exist—and will increase—in portable video equipment (cameras), imaging and graphics, communications (e.g., wireless LANs and modems), high speed instrumentation, data-acquisition, and surveillance systems.

In single-supply equipment, an especially useful application for amplifiers like the AD8011 is in buffering input sources from the A/D converters that they must drive. In Figure 3, the AD8011 is shown buffering and level-shifting a 0-to-1-volt input source for an AD876, a 10-bit, 20-MSPS, single-supply ADC (see page 19). The AD8011 circuit provides a gain of –2 and an offset voltage of 3.6 V to drive the AD876 with a 2.0-volt span from 3.6 V to 1.6 V for an input from 0 V to +1.0 V.

The input circuit of the AD876 is a MOSFET switch with R_{ON} of 50 Ω in series with a 5-pF capacitor. The additional 100-Ω resistor limits the maximum output current from the amplifier to about 13 mA for a full-scale 2-V output change, yet with a short enough time constant for the capacitor's charge to settle to within 10-bit accuracy well within the AD876's 25-ns sampling period.

The AD8011 was designed by Roy Gosser, of ADI's Standard Linear IC Division, at Greensboro NC. The XFCB process was designed and implemented by a team led by ADI Fellow Jody Lapham, at our fab facility in Wilmington MA.

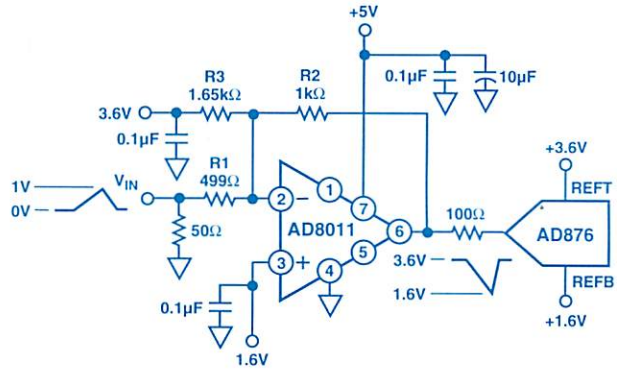


Figure 3. Driving the AD876 A/D converter.

*Use the reply card for technical data. **Circle 2**

Design Circuits with Digitally Controllable Variable Resistors

AD8402/3 dual/quad digital pots set resistance values and ratios remotely

by Walt Heinzer

Here is the first viable cost-effective substitute for trimmers and potentiometers in new designs. This new IC family offers digital control of the variable-resistance function. Basically a set of D/A converters in which resistance—or resistance ratio—is the analog variable, they are in contrast to (but complement) the family of TRIMDACs® (*Analog Dialogue* 24-3, 1990, pp. 16-18), which can be thought of as *buffered potentiometers*. The newer devices are controllable circuit elements—*variable resistors* (VRs) or *unbuffered pots*; for example, they allow users to directly program time constants and filter cutoffs in traditional R-C circuits.

The first of these, the 2-channel 8-bit (256 positions) AD8402 and 4-channel AD8403 (Figure 1), provide standard full-scale resistance values of 10 kΩ, 50 kΩ and 100 kΩ, with ±20% tolerance. A "wiper contact" taps the resistor (R_{AB}) at a point selected by the digital input. The resistance between the wiper and point B is nominally proportional to the stored digital code, and the resistance between the wiper and point A is proportional to its 2s complement (complement + 1 LSB). Requiring +3-V to +5-V single supplies to operate the switches, the devices are programmed by a 3-wire serial data interface that is compatible with many of the standard microcontroller serial buses, including SPI, QSPI and the Intel microcontroller serial data ports.

Ideal for low-power, battery-operated applications, these devices conserve power in several ways. The digital interface circuits use standard static CMOS logic, which dissipates power only during updates; once set, only nanoampere-level leakage currents flow. A digital *shutdown* mode open-circuits the variable resistor, reducing its current to zero. After the shutdown mode is ended, the previous setting is returned if the V_{DD} supply has not been interrupted. Another useful digital function, *midscale reset*, sets the device at mid-range when initially powered up; the controlled signal can then be adjusted up or down to a final value.

The AD8402/3 were designed to allow circuit *resistances* to be controlled remotely with precision. Previously, only currents, voltages, and gains could be controlled digitally (i.e., by DACs). For applications where simple resistance adjustments would be adequate, the use of complete DACs could lead to "overkill" in terms of circuit complexity, space, power, and cost.

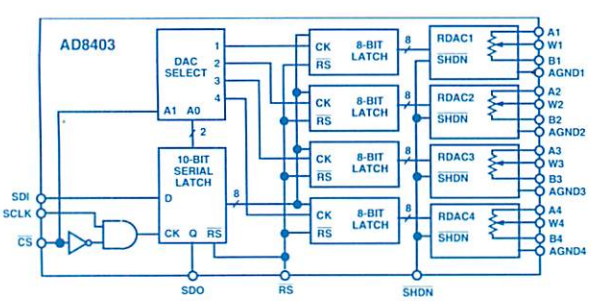


Figure 1. AD8403 Functional block diagram.

As portable circuit designs become ever-more-compact, pots are too big to fit; if used, they are hard to access. The >3-mm height of the smallest trimmers makes them impractical for many compact portable designs—for example, TYPE I PCMCIA-card circuit standards require all components to have a physical height <2 mm. The higher circuit density possible with digitally adjustable IC resistors resolves these space constraints, removes active signals from instrument front panels, reduces wiring costs, and makes it possible to save "front panel" settings in EEPROM.

Thus the digital potentiometer ("RDAC") provides the solution, with its compact 1.5-mm high SO-14 package and 256 settings. It can be located directly at the circuit point requiring adjustment to minimize noise pickup and simplify front-panel wiring. It is free from the problems of shock, vibration, and open-contacts that often disqualify pots. And it is programmable—settings can be saved in system memory for later recall. The three-terminal functionality—full access to both ends of the pot and the wiper—allow it to be employed in simple panning circuits. As a variable resistor, the AD8402/3 can be combined with capacitors for simple programmable time-constant adjustments in standard low-pass and high-pass filters for a variety of applications.

OPERATION

The two principal configurations of the RDAC are the 3-terminal potentiometric divider and the two-terminal rheostat. In Figure 2a, the open-circuit voltage, V_{WB}, is proportional to the digital input value. In 2b (A open), the resistor, R_{WB}, is proportional to the digital input (and is in series with 50-Ω contact resistance).

A few boundary conditions must be satisfied for proper operation of the AD8402/03: All analog signals must remain within the applied single-supply voltage range. For standard pot/divider applications, the wiper output can be used directly, but for low-resistance loads, buffer the wiper with a suitable rail-to-rail op amp, such as the OP291 or OP279, to maintain linearity and provide drive current. For ac signals and bipolar dc adjustments, an offset ground (e.g., a 2.5-V reference) will generally be needed. It must be able to handle any necessary sink and source current for all connected loads and bypass capacitors.

RDAC PARAMETRIC PERFORMANCE

The basic specs used in selecting any variable resistor include *nominal resistance*, *tolerance*, and *temperature coefficient* (TCR/tempco). The AD8402/3 are available in 10-kΩ, 50-kΩ and 100-kΩ standard values with ±20% tolerances. The nominal TCR at midscale is 500 ppm/°C, with a typical long-term drift of 0.1%.

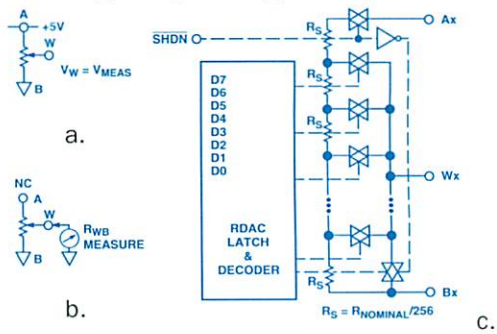


Figure 2. Equivalent circuits. a. Potentiometer divider: 3-terminal connection. b. Rheostat: 2-terminal connection. c. Equivalent RDAC circuit, showing $\overline{\text{SHDN}}$ switches.

In addition, the specs must include *resolution* (256 positions—8 bits), *operating supply range* (+3 to +5 V), and *position linearity*. For potentiometer divider applications, conventional DAC integral and differential nonlinearity specifications (INL and DNL) apply. For the rheostat, (as measured between the wiper and the end terminals), new parameter definitions (and associated test circuitry) were needed to define nonlinearity of the resistance step position value in relation to code. Modeled on INL and DNL, (test circuits are provided on the data sheet) they are:

- **R-INL**, *Resistor position integral nonlinearity*—the worst-case deviation from ideal value over the range from maximum-resistance to minimum-resistance wiper positions.
- **R-DNL**, *Resistor position differential nonlinearity*—compares the actual step change with the ideal, ($R_{WBfull\ scale}$/256) between successive tap positions.

The AC characteristics of the RDACs are dominated by the internal parasitic capacitances and the external capacitive loads. The *–3-dB bandwidth* of the AD8403AN10 (10-kΩ resistors) measures 600 kHz at half-scale as a potentiometric divider. The *total harmonic distortion plus noise* (THD+N) is measured at 0.003% in an inverting op-amp circuit using an offset ground and the rail-to-rail OP279 amplifier (Figure 3 left). *Thermal noise* is primarily Johnson noise, typically 9 nV/$\sqrt{\text{Hz}}$ for the 10-kΩ version at f = 1 kHz. *Channel-to-channel crosstalk* measures less than 65 dB at f = 100 kHz. To achieve this isolation, the extra ground pins provided on the package to segregate the individual RDACs must be connected to circuit ground. *Power supply rejection* is typically –35 dB at 10 kHz (care is needed to minimize power supply ripple in high-accuracy applications).

As noted earlier, special attention has been paid to device power consumption. After transient current flows at data changes, the internal logic consumes typical leakage currents of 10 nA at room temperature. The variable resistor will of course dissipate power whenever current is flowing through the wiper and terminals. The shutdown feature will asynchronously open-circuit the device (Figure 2c), stopping power dissipation in the variable resistor when the $\overline{\text{SHDN}}$ pin is asserted, without affecting the wiper position setting held in the RDAC latch. After exiting from shutdown, the wiper returns to its previous setting.

Both devices operate over the extended industrial temperature range, –40 to +85°C. The AD8402 is available in 14-pin plastic DIPs and SO; the AD8403 is available in a SOIC-24 package. 10, 50, and 100-kΩ options are designated by the digits at the end of the part number; e.g., AD8402AN10 is a 10-kΩ device in a plastic DIP.* Prices for AD8402/03 in 1000s are $1.66/$2.51.

APPLICATIONS

Figure 3a shows one channel of the AD8402 connected in an inverting wide-range programmable-gain op-amp circuit. The +2.5-V reference serves as an offset "ground", allowing the circuit's output to span a ±2.5-volt range, using the rail-to-rail OP279 amplifier. For gains >1 (code = 80_H), the digital input is increased toward code FF_H; for gains <1, the digital input is decreased toward code 00_H. The plot in 3b shows the wiper settings for a 100:1 range of voltage gain (V/V). Note the ±10 dB of pseudo-logarithmic gain around 0 dB. This circuit is mainly useful for gains from 0 V/V to 4 V/V; beyond this range, the step sizes become very large, and the resistance of the driving circuit can become a significant term in the gain equation.

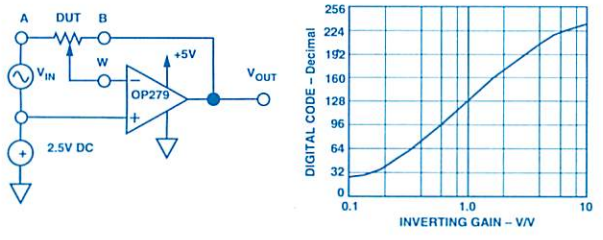


Figure 3. Inverting programmable gain amplifier and plot of settings for gains from 0.1 to 10 (log scale).

*For technical data and/or an AD8402AN10 sample, use the reply card. Circle 3 for data, 4 for sample.

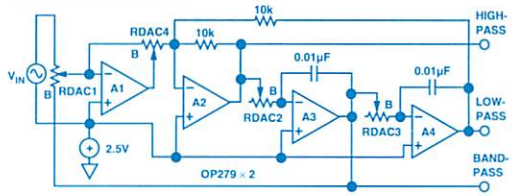


Figure 4. Programmable state-variable active filter.

Active filter: The state-variable filter circuit can simultaneously exhibit low-pass (LP), high-pass (HP), and bandpass (BP) filter characteristics; it is an analog computing circuit solving a second-order differential equation. Digital pots and resistors can be used instead of DACs to program frequency, gain, and Q (Figure 4).[1] The filter circuit uses a +2.5-V virtual ground, which readily allows up to 4-V p-p input and output swing for each stage.

RDACs 2 and 3 set the LP and HP cutoff frequencies—and the BP center frequency. With equal *C*s, they are programmed with equal data (like ganged pots) for best dynamic range. The bandpass gain depends only on RDAC1; then RDAC4 can be used to adjust the Q (which depends on RDAC1, RDAC4, and the ratio of RDACs 2 & 3). Figure 5a shows the measured BP filter response over a range of center frequencies from 2 kHz to 20 kHz. The filter gain response at the BP output is shown in Figure 5b, as RDAC1 adjusts the gain over a range of –20 to +20 dB at a center frequency of 2 kHz. As expected, circuit Q varies with gain. For more detailed reading on the state-variable active filter, see Analog Devices Application Note AN-318.

Adjustable timer: The AD8402, with a capacitor and a comparator, can produce programmable time-delayed switching after a step input. Similarly, the RDAC can be used to improve the accuracy of 555-timer circuits, such as a calibrated one-shot.

The AD8402/3 was designed by James Ashe at ADI's Santa Clara, CA, site.

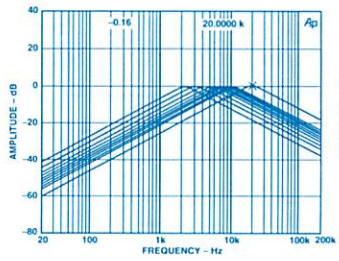


Figure 5a. Bandpass output vs. frequency at unity gain.

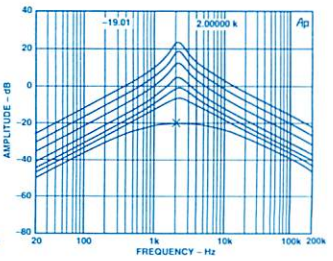


Figure 5b. Bandpass output over a gain-range of 100:1.

[1]See p. 247 ff., *Analog-Digital Conversion Handbook*, 3rd edition, Engineering Staff of Analog Devices, ed. by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall, 1986. Available from Analog Devices. [use book purchase card]

Micromachined Complete-on-a-Chip Sensor Measures ±5-*g* Accelerations

ADXL05 is a complete, low-cost monolithic 200-mV/*g* system for measuring acceleration

by Charles Kitchin

The ADXL05* is a new accelerometer designed to measure accelerations from a few m*g* up to its full-scale level of ±5 *g*. Requiring only 0.25 square inches of board space, and operating on a single +5-volt supply, the ADXL05 is pin-compatible with the ±50-*g* ADXL50 [*Analog Dialogue* 27-2], widely used in automotive airbag deployment. The ADXL05 is somewhat similar in design to the ADXL50, but its more-compliant beam suspension results in a nominal 200 mV/*g* sensitivity, 10.5× that of the ADXL50. The increased output greatly improves the ratio of signal to noise & drift when measuring low accelerations.

Accelerometers can be used in all sorts of dynamic measurements—and some static measurements—from muscular strength to arming missiles on impact and evaluating the quality of handling goods during shipment, as well as in car security systems, oil drilling rigs, toys, tanks, and automotive chassis motion control. Since the various applications differ in their acceleration ranges, the availability of accelerometers with both ±5-*g* and ±50-*g* ranges has greatly increased the possibilities available to the designer.

Like the ADXL50, the ADXL05 is a complete acceleration measurement system on a chip, fabricated in a process known as surface-micromachining, in which the movable sensor element is etched out of the same polysilicon die as the transistors and other components that make up the signal conditioning circuitry. The resulting die size is amazingly small—less than 10 mm^2—yet it includes all of the circuit elements necessary to provide a 0-5-V output signal that is linear, temperature-compensated, and proportional to positive or negative acceleration along the sensitive axis. Because everything is made on a single monolithic die, these tiny accelerometers can be mass-produced at low cost.

Figure 1 is a block diagram showing the required connections. Resistors R1 & R3 set the gain of the on-chip buffer amplifier to provide the desired output range. Optional resistor R2 can be added

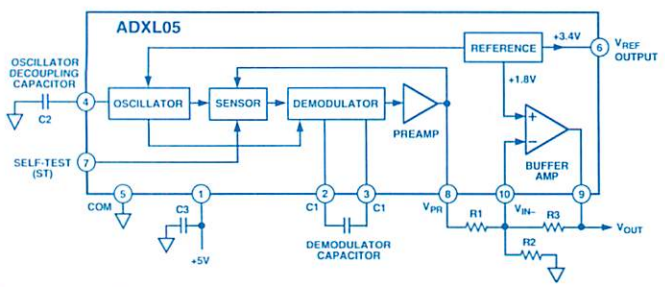
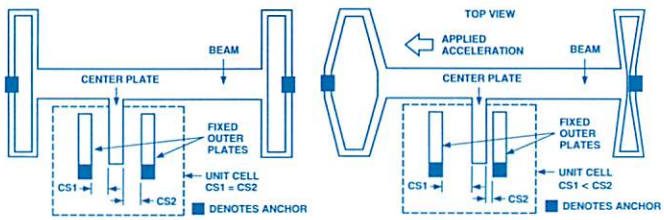


Figure 1. Functional block diagram of the ADXL05 and its external connections.

*For technical data on the ADXL05, use the reply card. Circle 5

to adjust the +1.8 volt 0-*g* offset level as needed (e.g., to +2.5 V for max ± range). Capacitors C2 & C3 provide oscillator decoupling and power-supply bypassing. Capacitor C1 sets the bandwidth of the feedback loop—and thus the upper-frequency measurement limit. In most applications, a few hundred Hz will be adequate. However, if necessary, the ADXL05 will support bandwidths up to 10 kHz. Low-pass filtering—to improve the signal-to-noise ratio or minimize aliasing in sampled-data systems when used with an A/D converter—can be implemented very easily by simply adding an external capacitor across resistor R3.

The accelerometer's on-chip 3.4-V reference is also available externally; and the buffer amplifier permits the user to modify the output sensitivity and 0-*g* voltage level. A self-test function allows device functionality to be verified at any time.



a. Sensor in unaccelerated condition: moving plate centered between fixed plates.

b. Sensor responding to leftward acceleration. Moving plate lags fixed plates, unbalancing capacitors.

Figure 2. How the the basic sensor works.

Figure 2a, a highly simplified view of the accelerometer's sensor element with no acceleration applied, shows the central beam with one of many paralleled movable plates attached, and one of many pairs of fixed plates. The actual plates are only 100 µm long—about 5 times the diameter of a human hair. The plates form a capacitive divider whose ratio changes when the central beam moves (at right angles to the plates).

The sensor's fixed capacitor plates are driven electrically by a pair of 1-MHz square waves of equal amplitude but 180° out of phase. At 0 *g*, the two capacitances are equal, and the voltage output at the divider tap (the central beam) is zero. In Figure 2b, the sensor responds to an applied acceleration. The beam moves closer to one of the fixed plates and farther from the other. This changes the ratio of the capacitances, producing an output signal at the central beam, increasing with the acceleration experienced by the sensor. The phase of the signal depends on the direction of beam motion, and synchronous demodulation produces a "dc" output of appropriate polarity. In actuality, the sensor feeds back this voltage to the plates to produce an electrostatic restoring force to balance the acceleration force so as to minimize the deflection of the center beam. The output voltage reflects the force required to keep the center beam essentially stationary ($F = ma$).

The ADXL05 will respond to gravity, showing + or –1 *g* when aligned with its sensitive axis vertical. Transverse response (to acceleration at 90°) is <2%. The ADXL05, housed in a TO-100 can, is available for commercial and extended-industrial temperature ranges. Pricing starts below $20.00 in 100s.

The ADXL05 design team at our Transportation and Industrial Products Division, Wilmington, MA was led by Kevin Chau.

About Ratiometric Converters

And a V_{out} temperature sensor that gets precise results with imprecise supplies

by Steve Martin

The output of an A/D converter is a digital number that represents the ratio of the input voltage to the reference voltage. If the reference voltage is furnished externally, the measurement is considered to be *ratiometric*. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference; but this implies that the signal to be applied to the converter is either the result of an absolute measurement, hence reference-independent, or somehow depends on a separate fixed reference.

However, real references are not truly fixed; the references for both the converter and signal source vary with time, temperature, loading, etc. This is not a problem where precision references are used; but precision references, whether internal or external, have their cost. So if the converter is used with signal sources that rely on proportionality to their references (e.g., strain-gage bridges, RTDs, thermistors, or the recently introduced AD22100 IC temperature sensor—to be described below), it makes economic sense to replace this multiplicity of references by a single system reference if reference-caused errors will tend to cancel out.

Figure 1 illustrates the principle with a buffered potentiometer measuring a position, K, and a sampling ADC. If the output of the potentiometer is $K \cdot V_{DC}$, with the digital output of the converter = $D(V_{IN}/V_{REF})$, and $V_{REF} = V_{DC}$, the converter output is simply $D(K)$, independently of V_{DC}.

This can be implemented using the converter's internal reference (if it has one that is available externally) as the system reference. Another way is to use a separate external system reference. This approach is most attractive, and quite easily implemented, when the *system power supply voltage* can be the system reference. It is especially useful—saving space, power, and cost—in battery-powered precision equipment, since supply voltage can be expected to vary from battery to battery and with temperature, time, and history.

PRECISION TEMPERATURE MEASUREMENT

For ratiometric applications involving temperature measurement within the range, –50 to +150°C, a new integrated-circuit device, the AD22100,* operating on +5-V (nominal) single supply, may be of especial interest. As Figure 2 shows, its basic architecture is similar to that of an RTD measuring system: A supply-dependent current is driven through the equivalent of a temperature-sensitive linear resistor, and the resulting voltage is amplified and offset to

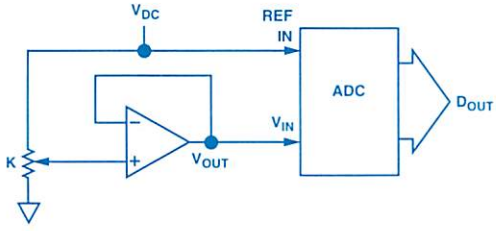


Figure 1. Illustration of ratiometric conversion.

*For technical data, use the reply card. Circle 6

embody the equation:

$$V_{OUT} = \frac{V+}{5\text{ V}}[1.375\text{ V} + T_A°\text{C} \times 22.5\text{ mV/°C}$$

whence one can interpret the readings as:

$$T_A(°\text{C}) = \frac{V_{OUT}\frac{5\text{ V}}{V+} - 1.375\text{ V}}{22.5\text{ mV/°C}}$$

With 5-V supply, at 650 µA max, the output of the AD22100 swings from +0.25 V to +4.75 V over the –50 to +150°C range. Accuracy and linearity errors are less than ±2% and ±1% of full scale. The AD22100, housed in plastic TO-92 and SO packages, offers three ranges with guaranteed specs, **S**: –50 to +150°C, **A**: –40 to +85°C, and **K**: 0 to +100°C. It is also available in chip form. Price for TO-92 versions, in 100s, starts at $1.21.

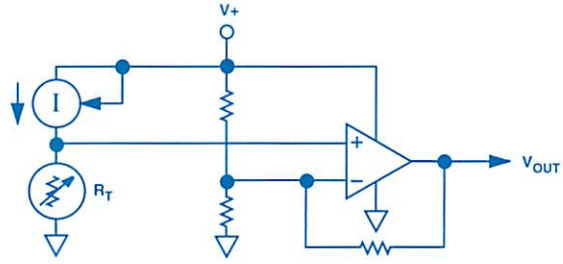


Figure 2. AD22100 temperature-sensor block diagram.

Figure 3 shows an example of a circuit in which the AD22100, used in conjunction with a single-supply A/D converter, such as the AD7820, is powered from the voltage applied to the converter's 5-V reference input. The conversion result is essentially independent of supply voltage changes and of drifts in the converter's reference voltage.

The AD22100 can be profitably used in heating, ventilating, air-conditioning (HVAC) systems, system temperature compensation, board-level temperature sensing, electronic thermostats, and countless other applications. The AD22100 is especially well-suited to providing a low-cost temperature-measurement capability for microprocessor/microcontroller-based systems. Many inexpensive 8-bit µPs now offer an onboard 8-bit ADC capability at a modest cost premium. Total "cost of ownership" then becomes a function of the voltage reference and analog signal conditioning necessary to interface the analog sensor with the µP's A/D converter.

The AD22100 can provide a low-cost temperature-measurement interface by eliminating the need for a precision voltage reference and any additional active-circuit components. Ratiometric conversion with the AD22100 allows the microprocessor's ADC reference to use the same basic power supply as the µP. Variations of hundreds of millivolts in the dc supply voltage have little effect.

The AD22100 was designed in Wilmington, MA, by Analog Devices Fellow Paul Brokaw.

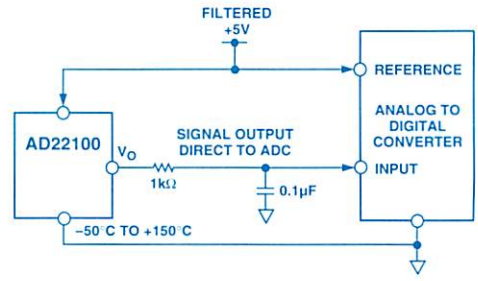


Figure 3. AD22100 in a ratiometric conversion application.

DSP Family Adds 3.3 V Operation, 8 K Words of On-Chip 24-Bit Program ROM

ADSP-2172 augments existing 2-K program RAM and 2-K data memory. ADSP-2173 has 20 MIPS with 10-MHz crystal at 3.3 V

The ADSP-2171, ADSP-2172, and ADSP-2173 are single-chip microcomputers* optimized for digital signal processing (DSP) and other high-speed numeric processing operations. The first of this family was the **ADSP-2171** (*Analog Dialogue* 28-1, 1994); it is being used for such applications as algorithm signal-processing for speech coding and soft-decision equalizing in GSM baseband processing—as well as low-delay code-excited linear prediction (LD-CELP), echo cancellation, and call processing for telephony. The **ADSP-2173** makes available the same functions with 3.3-V supplies (dissipating only 70 mW with a 10-MHz crystal and 360 µW in power-down); and the **ADSP-2172** adds 8 K words of 24-bit program custom ROM, making program downloading from a host unnecessary in many applications. The ADSP-2171 and ADSP-2172 provide 33-MIPS operation from a 16.67-MHz crystal with 5-V supply.

Figure 1 is a functional block diagram of the ADSP-2172, showing at left the well-known and proven ADSP-2100 16-bit fixed-point microprocessor base architecture, featuring three independent computational units: ALU, multiplier-accumulator, & shifter, two data-address generators, and program sequencer, with extensive interrupt capabilities (*Analog Dialogue* 20-2, 1986). It also shows additional features first made available in the ADSP-2101 DSP microcomputer (Analog Dialogue 23-2, 1989)—on-chip memory (2 K × 24-bit program RAM, 2 K × 16-bit data memory), serial ports, programmable timer, and a simplified external bus system. The newest additions—host interface port, powerdown control logic, and increased on-chip memory (8 K × 24-bit program ROM), can also be seen.

The ADSP-217x are code- and function-compatible with the ADSP-2100 family's powerful architecture and instruction set, which allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-217x can:

- generate the next program address
- fetch the next instruction
- perform 1 or 2 data moves
- update 1 or 2 address pointers
- perform a computational operation

while at the same time receiving and transmitting data through the two serial ports and the host interface port, and decrementing the timer. The ADSP-217x has new instruction-set enhancements for bit manipulation, multiplication, biased rounding, and global interrupt masking, for increased flexibility.

Support for the ADSP-217x is available in the form of the ADSP-2100 Family Development Software tools for hardware and software system development. In addition, EZ-Tools, low-cost, easy-to-use hardware tools, are also available: The ADSP-217x EZ-ICE® Emulator aids in hardware debugging of ADSP-217x systems, and the EZ-LAB® evaluation board, a PC plug-in card, can also operate in a stand alone mode.

The ADSP-217x are available in 128-pin TQFP and PQFP packages and are specified for operation over the 0 to +70°C and –40 to +85°C temperature ranges. Power-down circuitry is provided to meet the low-power needs of battery-operated portable equipment. Prices for 5-V/3.3-V units start at $32/$38 in 1000s. The EZ-LAB evaluation board is priced at $695, and the EZ-ICE's price is $1,995.

The ADSP-217x family was designed by a team led by Greg Koker and Steve Tsang at our Computer Products Division in Norwood, MA.

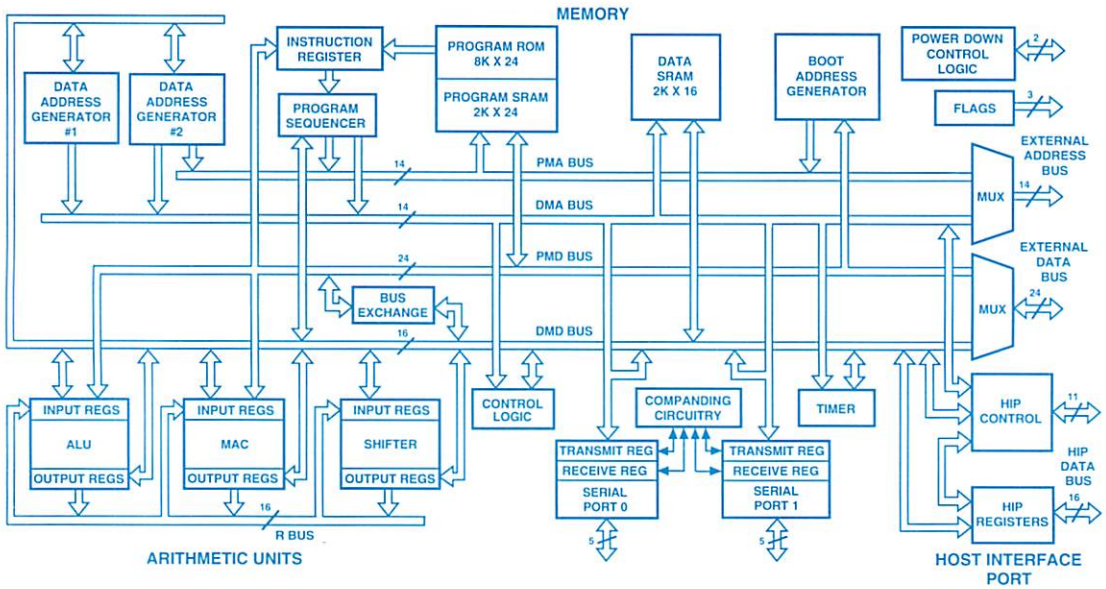


Figure 1. ADSP-2172 block diagram.

*Use the reply card for technical data. **Circle 7**

Understanding and Using High-Speed Clamp Amplifiers

A new architecture using input clamping is more versatile and accurate than output clamping

by Peter Checkovich

INTRODUCTION

A clamp amplifier is a limiting or bounding circuit. For input voltages between two levels, V_H and V_L, the output is proportional to the input. For inputs greater than V_H or less than V_L, the output ideally remains constant, bounded at V_{CH} or V_{CL} (V_H or $V_L \times$ the amplifier gain, A_V), irrespective of the input, as shown in Figure 1. The threshold voltages, V_H and V_L, may be fixed or can vary at speeds comparable to the speed of the input. If the amplifier can handle positive and negative input/output voltages, V_H and V_L can have any plus or minus values within the specified range, as long as $V_H > V_L$.

The AD8036 and AD8037 wide-bandwidth, low-distortion clamp amplifiers, introduced in the last issue (*Analog Dialogue* 28-3, pages 6 & 7),* are basically wideband voltage-feedback operational amplifiers with 175- and 180-MHz large-signal bandwidth. Between the + input terminal and the actual + input of the amplifier is a circuit that compares the applied input voltage with a pair of fixed or variable "clamp" voltages, V_H and V_L; if the input voltage is between the clamp voltages, it is chosen as the + input, otherwise, the appropriate clamp voltage is chosen.

Applications: The many potential applications for a fast, accurate, low-cost clamp amplifier are bounded only by the user's imagination. A variety of generic applications for limiters are described in the *Nonlinear Circuit Handbook*.† They can be used as buffers to prevent the application of overvoltage to downstream circuitry, such as A/D converters. They can be used in pulse forming and to provide accurate limits on pulse amplitude. Other uses include amplitude modulation, absolute-value computing (a k a full-wave rectification), and generating piecewise-linear and other discontinuous functions. Clamp-amp functions may be typically called for in such equipment as IF/RF signal processing, high-quality imaging, broadcast video systems, and instrumentation.

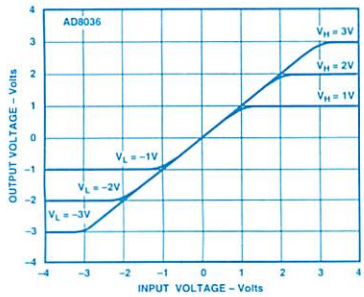


Figure 1. Clamp amplifier output-input characteristic at unity gain.

*For technical data, use the reply card. Circle 8

†*Nonlinear Circuits Handbook*, edited by D. H. Sheingold. Norwood, MA: Analog Devices, Inc., 1976. Available for purchase from Analog Devices. Use the book order card.

When controlled by external voltages, a clamp amplifier circuit is characterized by *linearity* (low distortion) in the unclamped range, *flatness* in the clamped range, *accuracy* of setting of the clamp voltages, and *sharpness* of the transition. Dynamically, when driven rapidly (viz., stepped) into the clamped zone, it must have low overshoot and quick recovery. If V_H and V_L are variable voltages, bandwidth must be adequate to handle them.

The AD8036 and AD8037 perform the clamp function with better performance than any available IC alternatives. Specifications include a clamp-voltage range of ±3.9 V (3.3 V min), clamp accuracy/flatness to within ±3 mV (5 mV max), a "knee" region of 100 mV. Maximum overshoot is 5% max in response to a 2× step overdrive, with recovery within 1.5 ns. The clamp input responds with a –3-dB bandwidth of 240 MHz, a useful feature when the clamp inputs are used to modulate an r-f signal.

To demonstrate how "clean" the clipping is, Figure 2 plots 2nd- and 3rd-harmonic distortion as a function of sine-wave amplitude as it approaches a ±1-V output clamp setting. The approach to the clamped region contributes no additional distortion for a >90% swing; and even *at the clamp threshold*, the worst distortion seen is only 1% (–40 dB).

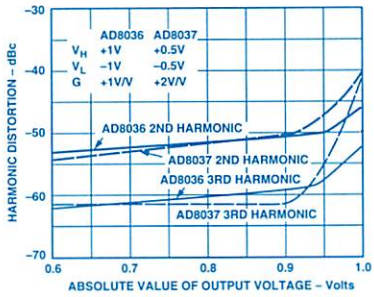


Figure 2. Clamp amplifier harmonic distortion as output amplitude approaches the clamp voltage. V_o = 2 Vp-p, R_L = 100 Ω, f = 20 MHz.

PERFORMANCE

The AD8036 and AD8037 are both wide bandwidth, low distortion clamping amplifiers. The **AD8036** is unity-gain stable. The **AD8037** is stable at gains ≥+2. Utilizing a unique patent-pending CLAMPIN™ input clamp architecture, the AD8036 and AD8037 offer a 10× improvement in clamp performance compared to traditional output clamping devices. In particular, clamp error is typically 3 mV or less and distortion in the threshold region is minimized. They can serve classical op-amp functions or as clamp amplifiers where high- and/or low output voltage bounds are specified or needed.

In the linear range, AD8036 and AD8037, which utilize a voltage feedback architecture, meet the requirements of many applications which previously depended on current feedback amplifiers. The AD8036 and AD8037 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%), wide small-signal and large-signal bandwidths, and very low distortion. The AD8036's distortion is –66 dBc at 20 MHz, with bandwidths of 240 MHz small-signal and 195-MHz large-signal. The AD8036 and AD8037 recover from 2× clamp overdrive within 1.5 ns. These characteristics position the AD8036/AD8037 ideally for driving as well as buffering flash- and high-resolution ADCs.

CLAMPIN is a trademark of Analog Devices, Inc.

In addition to traditional clamp amplifier applications, the input clamp architecture treats the clamp levels as additional inputs to the amplifier. Signals with speeds from dc up to 240 MHz can be applied to the clamp pins. The clamp values can be set for any value within the output voltage range, with the constraint that V_H is greater that V_L. The clamp characteristics make it possible to use the AD8036 and AD8037 in non-traditional applications such as a full-wave rectification, pulse generation, and amplitude modulation.

Both devices are offered in plastic DIP and SOIC versions for the industrial (–40 to +85°C) temperature range; and the AD8036 is also available in cerdip for the military (–55 to +125°C) temperature range. They are also available as chips. Industrial versions are priced at $4.12 in 1000s.

THE LINEAR MODE: CLAMP AMP AS AMPLIFIER

The AD8036 and AD8037 are wide bandwidth, voltage feedback amplifiers. Since their open-loop frequency response follows the conventional 6 dB/octave roll-off, their gain-bandwidth product is basically constant—increased closed-loop gain results in a corresponding decrease in small-signal bandwidth. The gain-bandwidth of the AD8037 is about twice that of the AD8036, which is compensated to be stable at a closed loop gain of +1. The AD8036/AD8037 typically maintain 65 degrees of phase margin, which minimizes the effects of signal and noise peaking.

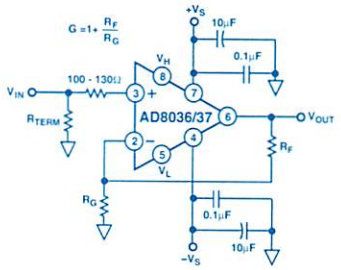


Figure 3. Typical connections for noninverting operation with gain.

Feedback resistor choice: The value of feedback resistance is critical for optimum performance of the AD8036 at gain = +1 (and less critical for higher gains). The AD8036 provides optimum unity-gain dynamic performance—the best combination of wide bandwidth, low parasitic peaking, and fast settling time—with R_F = 140 Ω. This resistor acts as a parasitic suppressor against damped RF oscillations that can occur due to lead inductance (input, feedback) and parasitic capacitance.

For similar reasons, a 100 to 130-Ω resistor should be placed in series with the positive input for other AD8036 noninverting configurations. The correct connection is shown in Figure 3.

For general voltage gain applications at higher gains, the amplifier bandwidth can be closely estimated as:

$$f_{-3\,dB} \approx \frac{f_0}{1+\frac{R_F}{R_G}}$$

where f_0 is the nominal unity-gain bandwidth. Small-signal frequency response for both amplifiers at closed-loop gains of +1 (AD8036) and +2 (AD8037) depart from this formula, as shown in Figure 4, as a function of feedback resistance, R_F.

Pulse response and large-signal performance: Unlike a traditional voltage-feedback amplifier, whose slewing speed is

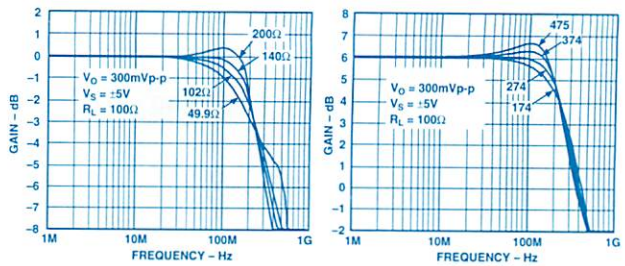


Figure 4. Small-signal frequency response. a. AD8036 (G = 1). b. AD8037 (G = 2)

dictated by its front end dc quiescent current and gain-bandwidth product, the AD8036 and AD8037 provide "on-demand" current that increases in proportion to the input "step" signal amplitude. The resulting slew rates (1200 V/µs) are comparable to those of wideband current-feedback designs—but with relatively low input noise current (2.1 pA/$\sqrt{\text{Hz}}$). The AD8036 and AD8037 combine the best attributes of both voltage- and current-feedback amplifiers. The outstanding large-signal operation (160 MHz min) of the AD8036 and AD8037 is due to a unique, proprietary design architecture, which limits the voltage-bandwidth product to 350 V-MHz (e.g., @ 100 MHz, $V_O \leq 3.5$ V p-p).

INPUT CLAMPING OPERATION

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their unique CLAMPIN input clamp architecture (patent pending). This new design reduces clamp errors by more than 10× over circuits that are based on output clamping, and substantially increases the bandwidth, precision, and versatility of the clamp inputs.

Figure 5 is an idealized block diagram of the AD8036 connected as a unity-gain voltage follower. The primary signal path consists of A1 (a 1200-V/µs, 240-MHz high voltage gain, differential to single-ended amplifier with dc gain of 1000 V/V) and A2 (a G = +1 high-current-gain output buffer) in cascade. The AD8037 differs from the AD8036 only in that A1 has a dc gain of 2000 and is optimized for closed-loop gains of two or more.

The key to CLAMPIN is the pair of comparators, C_H and C_L, which drive switch S1 through a decoder. The unity-gain buffers in cascade with the $+V_{IN}$, V_H, and V_L inputs isolate the input pins from the comparators and S1 without reducing bandwidth or precision. The two comparators have bandwidth comparable to that of A1 (240 MHz), so that they can keep up with signals within the useful bandwidth of the AD8036.

When V_{IN} is between V_H and V_L, C_H and C_L are both high, and S1 chooses V_{IN} at position A. When V_{IN} is greater than V_H, C_H goes low and S1 chooses V_H at position B; and when V_{IN} is less than V_L, C_L goes low and S1 chooses V_L at position C.

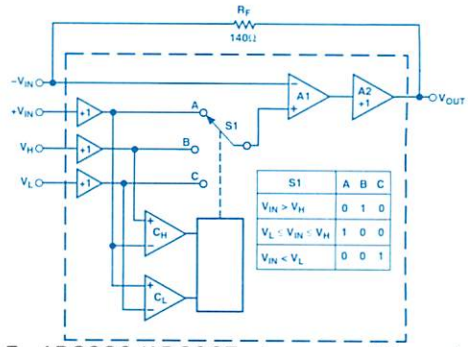


Figure 5. AD8036/AD8037 clamp amplifier principle.

To illustrate the operation of the CLAMPIN circuit, consider the case where V_H is connected to a 1-V reference, V_L is open or connected through a resistor to the negative rail, and the AD8036 is set for a gain of +1, by connecting its output back to its inverting input through the recommended 140-Ω feedback resistor. Note that the main signal path via the closed loop is unaffected by the clamp status, since the CLAMPIN circuit only affects A1's noninverting input. If a ramp voltage varying from 0 V to +2 V is applied to the AD8036's $+V_{IN}$, V_{OUT} should track $+V_{IN}$ perfectly up to +1 V, then should limit at exactly +1 V as $+V_{IN}$ continues to +2 V.

In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1 V, the output of the high-limit comparator, C_H, starts in the off state, as does the output of C_L. When $+V_{IN}$ just exceeds V_{IN} (ideally by < 1 μV, practically by about 18 mV), C_H changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to V_H, further increases in $+V_{IN}$ have no effect on the AD8036's output voltage. In fact, the AD8036 is now operating as a unity-gain buffer for the V_H input, and any variation in V_H, for $V_{IN} > V_H$, will be faithfully reproduced at V_{OUT}.

Operation of the AD8036 for low or negative input voltages is similar, with comparator C_L controlling S1. The comparators respond in complementary fashion to the voltage on the $+V_{IN}$ pin as their common reference level. For example, if V_L is at +1 V and V_H is open or at the + rail, for any value of $V_{IN} < +1$ V, comparator C_L will switch S1 to "C," so the AD8036 will buffer the voltage on V_L and ignore $+V_{IN}$.

The performance of the AD8036 and AD8037 closely matches the ideal. The comparator's threshold extends from 60 mV inside the clamp window defined by the voltages on VL and VH to 60 mV beyond the window's edge. Switch S1 is make-before-break, implemented with current steering, so that A1's +input makes a continuous transition from, say, V_{IN} to V_H as the input voltage traverses the comparator's input threshold from 0.9 V to 1.0 V for V_H = +1.0 V.

The practical effect of these nonidealities is to soften the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the CLAMPIN circuit. Figure 6 is a graph of V_{OUT} vs. V_{IN} for the AD8036, compared with a typical "output" clamp amplifier (one which performs clamping after comparing V_{OUT} with V_H). Both amplifiers are set for G = +1 and V_H = +1 V.

The worst-case error between V_{OUT} (ideally clamped) and V_{OUT} (actual) is typically 18 mV, multiplied by the amplifier's closed-loop gain. This occurs at $V_{IN} = V_H$ (or V_L). As V_{IN} goes above and/or below this limit, V_{OUT} will settle to within 5 mV of the ideal value.

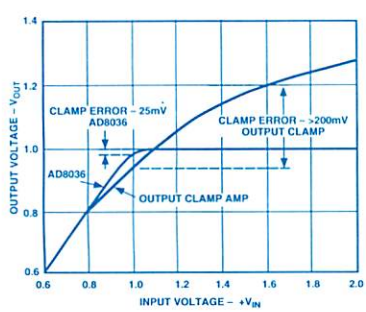


Figure 6. Comparison of typical errors of input clamp and output clamp.

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8 V, but the actual clamped value of output voltage can be as much as 200 mV beyond the clamp limit. In addition, since the output clamp, in effect, causes the amplifier to operate open loop while clamped, the amplifier's output impedance will increase, potentially causing additional errors.

The AD8036 and AD8037 can be used as amplifiers in either an inverting or noninverting configuration, with the positive input voltage determined by the CLAMPIN circuit (the clamp function will only work with noninverting inputs). However, there are applications in which the inverting connection is a useful adjunct; some will be shown below. In applications that do not require clamping, Pins 5 and 8 (respectively V_L and V_H) may be left floating or tied to the low and high rails through resistors.

Since the AD8036's and AD8037's CLAMPIN input clamp architecture is applied at the + input, V_H and V_L must be set at (1/gain) times the desired level to obtain a desired output clamp level. Input error limits will be magnified by the amplifier's closed-loop gain. For instance, to set an output limit of ±1 V for an AD8037 operating at a gain of 3.0, V_H and V_L would need to be set to +0.333 V and –0.333 V, respectively, and the threshold error would be tripled at the output.

The only restriction on input voltage applied to the devices' $+V_{IN}$, V_L, and V_H pins is that the maximum voltage difference between $+V_{IN}$ and V_H or V_L not exceed 6.3 V, and all three voltages must be within the supply-voltage range. For example, if V_L is to be set at –3 V, V_{IN} should not exceed +3.3 V.

APPLICATIONS

The AD8036/8037's unique approach to input clamping provides better clamping than do traditional output-clamping devices, with additional flexibility to perform some interesting applications. But there are some constraints on circuit configurations; and some simple calculations need to be performed to refer output clamping levels back to the input. Since clamping is applied only for noninverting applications, an additional inverting amplifier is necessary to clamp and invert or invert and clamp. Another constraint, mentioned earlier, is that V_H be more positive than V_L, and that both be within the output voltage range of the amplifier (±3.9 V). V_H can go below ground and V_L can go above ground as long as V_H is kept more positive than V_L.

Clamping with gains of +1 and +2: The simplest clamp circuit is a unity-gain follower, as shown in Figure 7a. In this case, the AD8036 should be used since it is compensated to be stable for G = +1. This circuit will clamp at an upper voltage set by V_H (the voltage applied to Pin 8) and a lower voltage set by V_L (the voltage applied to Pin 5).

Figure 7b shows an AD8037 configured for a noninverting gain of two. The AD8037 is used in this circuit, because it is compensated for gains ≥2 and provides wider bandwidth than AD8036. In this case, the high clamping level at the output will occur at $2 \times V_H$ and the low clamping level will be $2 \times V_L$. The equations governing the output clamp levels in circuits configured for noninverting gain (assuming zero offset) are:

$$V_{CH} = G \times V_H$$

$$V_{CL} = G \times V_L$$

where:

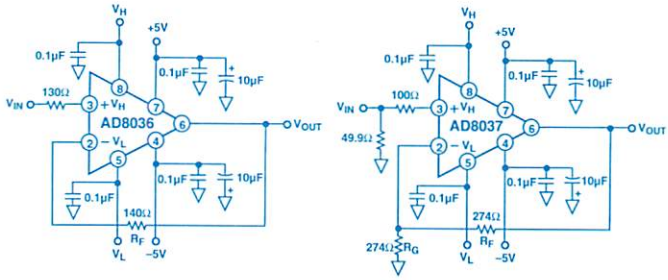
V_{CH} is the high output clamping level

V_{CL} is the low output clamping level

G is the gain of the amplifier configuration

V_H is the high input clamping level (Pin 8)

V_L is the low input clamping level (Pin 5)



a. AD8036 connected for unity gain.

b. AD8037 connected for gain of 2.

Figure 7. Noninverting circuits.

Programmable pulse generator: The AD8036/AD8037's clamp output can be set accurately and has a well-controlled flat level. Combining this with wide bandwidth, high slew rate, and low overshoot, they are well suited for programmable-level pulse generators. Figure 8 is a schematic of a pulse generator that can directly accept TTL timing signals at its input and generate output pulses of up to 24 V p-p with 2500 V/µs slew rate. The output levels can be programmed by V_H and V_L to any voltages in the range from –12 to +12 V.

The circuit uses an AD8037 operating at a gain of 2 V/V, followed by an AD811 connected for gain of 5 V/V to boost the output to the ±12-V range. The AD811 was chosen for its ability to operate with ±15 V supplies, its high output-current capability, and its high slew rate.

R1 and R2 act as a level shifter to approximately center the TTL signal levels about ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled output signal levels, the high and low output levels should result from their being clamped by the AD8037 and not be just a high or low logic level passing through a linear amplifier. For good, square rise- and fall times at the output pulse, a logic family with high-speed edges should be used.

The high logic levels are clamped at $2 \times V_H$, while the low logic levels are clamped at $2 \times V_L$. The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be $10 \times V_H$, and the low output level to be $10 \times V_L$.

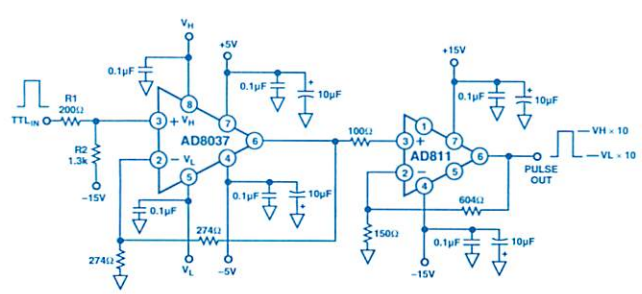


Figure 8. Programmable pulse generator.

High speed full-wave rectifier: The clamping inputs are additional inputs to the input stage of the op amp. As such they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 9 is a schematic for a full-wave rectifier, sometimes called an absolute-value generator. It works well up to 20 MHz and can operate at significantly higher frequencies with some degradation in performance. The distortion is significantly lower than that of diode-based full-wave rectifiers, especially at high frequencies. Full wave rectifiers are useful in many applications including AM signal detection, high-frequency ac voltmeters and various arithmetic operations.

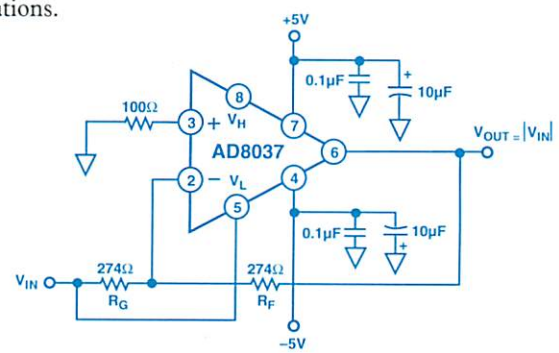
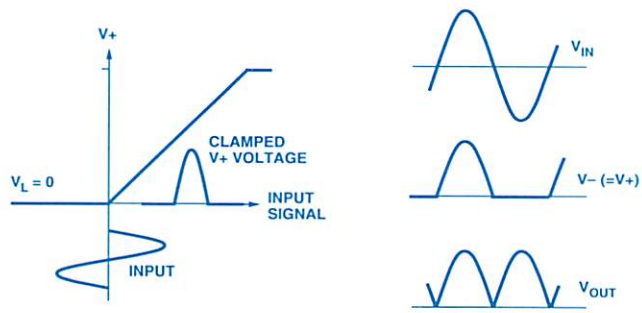


Figure 9. Full-wave rectifier circuit.

The circuit is configured as a unity-gain inverting amplifier. The input drives the inverting amplifier, and it also directly drives V_L, the lower-level clamping input. The high-level clamping input, V_H, is left floating and plays no role in this circuit, and the + input is grounded. The + input voltage to the amplifier (after the clamping circuit) is zero when the signal is negative, and follows the signal when it is greater than zero (Figure 10a).



a. V+ versus input transfer characteristic ($V_L = 0$).

b. Ideal waveforms.

Figure 10. Full-wave rectifier principle.

The feedback action of the operational amplifier causes the output to be whatever is necessary to maintain the – input equal to the + input. So, when the input is negative (+ input zero), the amplifier acts as a regular unity-gain inverting amplifier and outputs a positive signal at the same amplitude as the input. When the signal is positive, the amplifier's inputs are equal to the signal, so no net current can flow through the feedback circuit; this can only happen if the output is also equal to the signal (i.e., the amplifier behaves like a unity-gain follower).

Thus, the output is always positive, with a gain of |1|, whether the input is positive or negative (Figure 10b). The circuit can be easily configured to produce the negative absolute value of the

input by applying the input to V_H instead of V_L. Because the amplifier is only feeding back one-half of its output, (closed-loop gain of 2) the AD8037, with its wider bandwidth, can be used to advantage. Figure 11 is an actual response of the circuit to a 20-MHz, ±1-V sinusoidal signal. The frequency-doubling effect of full-wave rectification can be seen, but the sharp cusps do not appear because of rounding at the clamp threshold. There is also some attenuation of the higher harmonics.

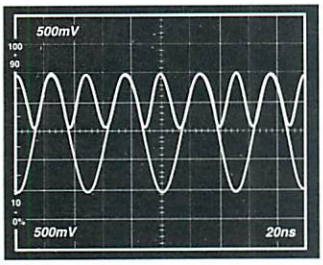


Figure 11. Full-wave rectifier input and output waveforms, showing frequency doubling.

The output can get to within about 40 mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range and is a result of the switching between the conventional op amp input and the clamp input. However, because there are no diodes required to rapidly switch from forward to reverse bias, the performance far exceeds that of diode-based full wave rectifiers. The 40-mV offset can be removed by adding an offset to the circuit. A 34-kΩ input resistor to the inverting input from either 5-V supply (depending on the polarity of the rectifier) will produce an opposing 40-mV offset, while affecting the gain of the circuit by less than 1%.

Amplitude Modulator: In addition to its use as an amplitude demodulator (AM detector), the AD8037 can also be configured as an amplitude modulator as shown in Figure 12. In this figure, a high-frequency carrier is modulated by a lower frequency signal.

The positive input of the AD8037 is driven by the carrier, a square wave of sufficient amplitude to produce clamping action at both the high and low levels.

The modulation signal is applied to clamping input, V_L, and to the input resistor of the unity gain inverting amplifier connection. Upper clamping input, V_H, is biased at +0.5 V dc.

Figure 13 shows the envelope waveforms in this circuit; the square carrier, V_C, is two-valued—a high value and a low value form the carrier's envelope. At the amplifier's "real" + input—after the clamps—the top of the carrier is clipped at +0.5 V; the bottom of the carrier is clipped by the modulation signal (V_M), to produce the envelope labeled V+. As in the case of the rectifier, the output is constrained by negative feedback to make the voltage at the – input ideally duplicate the voltage at the + input.

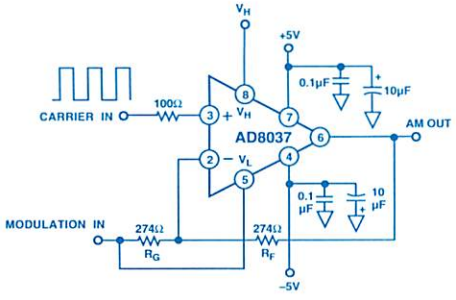


Figure 12. Amplitude modulator.

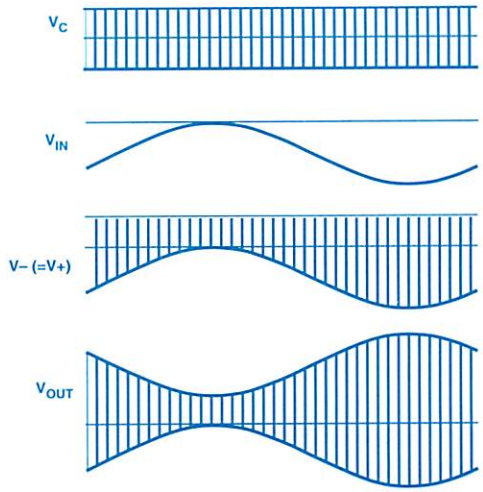


Figure 13. Waveforms in modulation circuit.

As with the rectifier, when V– is at the lower carrier value, equal to the modulation waveform, the output's lower envelope must duplicate this. But when V+ is at the upper carrier value, the modulation envelope is inverted and added to the constant 0.5 V.

The modulation index can be modified by changing the amplitude of the modulation signal; this changes the amplitude of the upper and lower envelope waveforms. The modulation index can also be changed by changing the dc bias applied to V_H; the amplitudes of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

LAYOUT CONSIDERATIONS

To achieve the specified high-speed performance of the AD8036 and AD8037 requires careful attention to proper RF design techniques, including board layout and component selection.

- The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path. However, the area near the input pins should be free of ground plane to reduce stray capacitance.
- Chip capacitors (0.01 to 0.1 μF) should be used to bypass supply and fixed-input clamp pins (see Figure 12). One end should be connected to the ground plane, the other within 1/8" of each power and clamp pin. An additional 0.47 to 10-μF tantalum electrolytic capacitor should be connected in parallel, though not necessarily so close, to handle large load-current transients. Some brands of electrolytic capacitors will require a small series damping resistor ≈4.7 Ω for optimum results.
- The feedback resistor should be located close to the inverting input pin to minimize stray capacitance at this node. Capacitance variations smaller than 1 pF at the inverting input will significantly affect high-speed performance.
- Stripline design techniques should be used for long signal traces (>1"), with a characteristic impedance of 50 or 75 Ω and properly terminated at both ends.
- When the AD8036/8037 must drive capacitive loads > 6 pF, a small series resistor will help preserve stability.

Carefully laid out and -tested evaluation boards for the AD8036 and AD8037 are available to demonstrate the high speed performance of the device. They are identified as AD8036EB & AD8037EB. They are priced at $37.50.

New Product Briefs (For information use reply card or see back cover)

Amplifiers: μpower, Logarithmic, Rail-Rail FET, Wideband

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Low-power OP193 specified at +2, +3, +5, and ±15 V

The OP193 single-supply op amp operates from voltages as low as +1.7 V to +36 V (or ±0.85 to ±18 V), with very low power and high precision—75-μV offset, low drift, high gain, and minimal phase reversal. It is ideal for designs that need long battery life: safety monitors, portable electronics, and medical instrumentation.

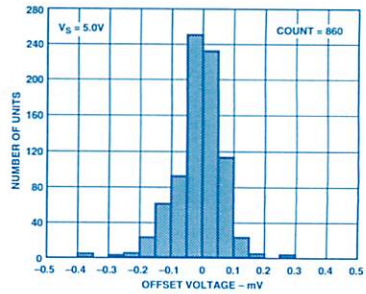
The OP193 draws only 15 μA of supply current, yet its outputs can sink and source ±8 mA. With its low power requirements, it continues to perform long after battery drain or limited headroom have made other amplifiers quit. The unity-gain-stable OP193 has dc open-loop voltage gain of 600,000 V/V and 35-kHz gain-bandwidth. Two performance grades are available for the –40 to +125°C range in a choice of 8-lead plastic DIPs or SOICs. Prices start at $1.37 in 1000s. **Circle 9**

Quad JFET Single-Supply Op Amp

AD824: first to combine low noise & bias current Rail-to-rail output, operates from +3 to ±15 V

The AD824 comprises four operational amplifiers, each with low bias current and current noise due to junction-FET input transistors. It is specified for operation at +3 V, +5 V, and ±15 V; and its outputs swing to within millivolts of the supply rails. The AD824 is extremely well suited for portable instrumentation applications, such as medical equipment, computer tomography, and computer peripherals.

The maximum bias current is 12 pA, and offsets are below 300 μV (at 25°C, +3 V and +5 V). The AD824 requires only 500 μA of quiescent current per channel, yet, despite its low-power operation, it has a very healthy 2-MHz gain-bandwidth product and 2-V/μs slew rate. The input stage allows the input voltage to safely extend beyond the negative supply and up to the positive supply rail without any phase inversion or latchup. The



outputs can sink or source 10 mA and are stable driving capacitive loads of up to 350 pF.

Two performance grades are offered to meet different offset voltage requirements. Both grades are available in 14-lead plastic DIP and narrow 14-lead SO packages for the –40 to +85°C extended industrial range. Prices start at $3.38 in 1000s. **Circle 10**

250-MHz Log Amp

AD641 complete wide-range demodulating amplifier

The AD641 is a logarithmic amplifier with a 44-dB dynamic range for frequencies from dc to 250 MHz. Based on the successive-detection principle used for the AD640 (*Analog Dialogue* 23-3, 1989), its output current is proportional to the log of the input voltage, at 1 mA/decade, with ±2-dB log conformance. Two AD641s can be cascaded for a 58-dB dynamic range. On-chip resistors can be used to scale output voltage, e.g., 37.5 mV/dB.

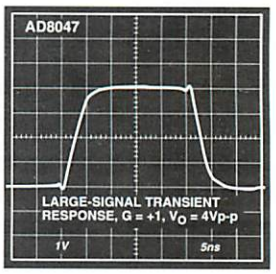
The AD641 compresses wide-range input signals for IF/RF signal processing, received-strength indicators (RSSI), ECM/radar, etc. It uses ±5-V supplies, and has an on-board ×10 range-shift attenuator. It is available for –40 to +85°C (20-pin plastic DIPs and PLCCs) and –55 to +125°C (cerdip). Prices start at $19.95 in 1000s. **Circle 11**

Low Power 250-MHz Op Amps

AD8047/AD8048 have 0.01% Δ gain, 0.02° Δ phase, 130-MHz large-signal BW, 30 ns to 0.01% settling

The AD8047 and AD8048 are high-speed, low-noise, wide-bandwidth voltage-feedback amplifiers that combine the best features of voltage feedback with some of the performance advantages of current feedback. The **AD8047** is unity-gain stable, with bandwidths of 250 MHz small-signal and 130-MHz large-signal (2 V p-p); while the **AD8048** is stable at closed-loop gains of 2 or more with bandwidths of 260 MHz and 160 MHz.

Though drawing low quiescent power (6.6 mA max on ±5-V supplies), they exhibit fast and accurate pulse response (30 ns to 0.01%) and low distortion (–54 dBc at 20 MHz: AD8047). They can drive 50 mA of output current (130 mA short-circuit); and capacitive loads up to 50 pF can be driven without normally requiring series resistance.



They are near-ideal for buffering high-speed ADCs, for a variety of speeds and resolu-tions: 12 bits to 10 MSPS or 8 bits to 60 MSPS. The balanced high-impedance inputs typical of voltage feedback allow maximum flexibility in active-filter design. Applications for them are many, including IF/RF, pulse, and video amplification, and DAC I/V buffers. They are available in 8-pin mini-DIP and SO for the –40 to +85°C range. Price in 1000s is $2.33. **Circle 12**

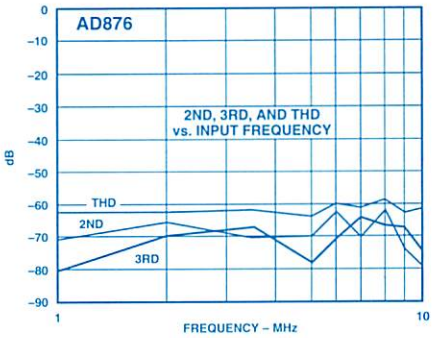
A/D Converters, Analog Muxes, Temperature Sensors

10-Bit, 20-MSPS Sampling ADC

Single-supply AD876 has low power consumption, High performance/low price for video, CCD, set-top

The AD876 is a 10-bit, 20-MSPS A/D converter with low power consumption (160 mW) for single supply-voltage (5-V) applications. A multistage pipelined architecture with output error-correction logic provides accurate performance and guarantees no missing codes over the full 0 to 70°C operating range. It is available in a 28-pin SOIC and 48-pin thin quad flatpack (TQFP). A pin-compatible 8-bit version is available for less-demanding, but upgradeable, applications. Prices (1000s) start at $9.95/$5.07 (10/8 bits).

Typical dynamic performance includes 150-MHz full-power bandwidth and –62 dB THD, 56-dB S/(N+D), and 65-dB SFDR at 3.58 MHz with 20-MSPS clock. The AD876's digital I/O interfaces to either 5-V or 3.3-V logic, and the output pins can be set to high impedance (i.e., 3-stated). A standby mode reduces power to less than 50 mW.



The AD876's speed, resolution, low power, and single-supply operation ideally suit a variety of fixed and portable applications in video, multimedia, imaging, high-speed data acquisition, and communications. Its speed and resolution make it suitable for systems with CCD inputs, such as color scanners, digital copiers, camcorders, and electronic still cameras. **Circle 13**

Protected Muxes

Faults, overvoltage ≤50 V 8:1 & 2×4:1, ADG438F/439F

The ADG438F and ADG439F are high-performance fault-protected multiplexers with overvoltage protection for signals from –35 V to +50 V. They are specified for operation over an extended temperature range, –40 to +105°C, and are available in narrow-body 16-lead SOICs and plastic DIPs. The **ADG438F** selects among 8 channels, and the **ADG439F** is a dual 4-channel (or 4-channel differential) mux.

The fault protection ensures that all channels are off if the power supplies are disconnected; and the ON channel is off while an overvoltage exists. This means that downstream devices, as well as the MUX, are protected against overvoltage and power loss. The switches are break-before-make, with t_{ON} of 250 ns max and t_{OFF} of 150 ns max. Either device in either package is priced at $4.35 in 100s. **Circle 14**

Sensor-Input ADC

24-bit AD7711A has PGA, 400-μA RTD excitation

The AD7711A is a complete 24-bit oversampling A/D converter for acquiring sensor information directly from resistance temperature detectors (RTDs) and voltage sources. It furnishes 400 μA of excitation current to an RTD or other resistive transducer. An on-chip PGA, with gains from 1 to 128, is programmed to provide any needed gain and to optimize the converter's input range.

The device includes a programmable low-pass filter, a bidirectional serial interface for microcontrollers, the ability to read/write calibration coefficients, and an available on-chip 2.5-V reference. Only 25 mW is required from a 5-V single supply (7 mW in Standby). Availability is in 24-lead SOIC for –40 to +85°C and cerdip for –55 to +125°C. Price (SOIC, 1000s) is $15.30. **Circle 15 for data sheet, 39 for sample**

12-bit, 10-MSPS A/D

AD872A: <noise, nonlinearity Dynamic specs 3-dB better

The AD872A is an improved-performance version of the AD872 monolithic 12-bit, 10-MSPS sampling A/D converter (*Analog Dialogue* 27-1, 1993, p. 22). Typical RMS noise has been reduced by one-half, differential and integral nonlinearity by 30%, and dynamic specs have been improved by from 2 to 5 dB, as the table shows (10-MSPS Sampling):

	AD872		AD872A	
Parameter	**1 MHz**	**5 MHz**	**1 MHz**	**5 MHz**
S/(N+D),dB	63	63	68	66
THD, dBc	–70	–70	–74	–72
SNR, dB	64	64	69	67
SFDR, dB	72	70	75	74

Pin-compatible with the AD872, the AD872A has the same dissipation, ≤1.3 W max. It is available packaged in ceramic DIPs and LCCs, for both 0 to 70°C and –55 to +125°C ranges. Prices start at $165 in 100s. **Circle 16 for data sheet, 40 for sample**

3.3-V Temp. Sensor

Voltage-output AD22103: on-chip signal conditioning

The AD22103 is a monolithic 3-terminal single-supply temperature sensor with on-chip signal conditioning and low-impedance voltage output proportional to the supply (28 mV/°C with a +3.3-V supply). Its 0 to 100°C span is useful in many applications, including thermal management, portable electronic equipment, and instrumentation.

Its patented circuit measures and conditions the voltage developed across a temperature-sensitive resistor with constant-current excitation. The ratiometric, rail-to-rail output provides a cost-effective solution with an A/D converter, using the ADC's reference as the AD22103's supply. Accuracy and linearity are better than ±2.5% & ±0.5% of full scale. It is housed in a plastic TO92 package and 8-lead SOIC. Price (1000s) starts at $1.17. **Circle 17**

Signal processors, DDS evaluation, Supervisory circuits

Signal Processors

ADSP-21msp58/59: 26-MIPS DSP + ADC, DAC

The ADSP-21msp58/59 are high-performance fully integrated mixed-signal processors. They combine, on a single CMOS chip, a 26-MIPS general-purpose signal-processing core like that of the ADSP-2171, 16-bit A/D and D/A converters, and signal-conditioning circuitry. Both devices are housed in 100-pin PQFPs and contain 2K 24-bit words of on-chip *program* memory RAM plus 2K 16-bit words of on-chip *data*-memory RAM. The **ADSP-21msp59** contains in addition 4K words of on-chip program-memory *ROM*. Communication facilities include an 8-bit host-interface port (HIP) and two double-buffered serial ports with companding hardware.

These processors are useful where voiceband analog signals need to be processed digitally in designs for which the space and cost of using separate DSP and codec components are excessive. Examples include analog cellular and digital mobile radios, personal computers, telephone answering machines, voice-mail systems, personal pagers and pay phones.

The ADSP-21msp58/59 use the proven ADSP-21xx 16-bit fixed-point architecture and are fully code-compatible for users familiar with other members of the family. The high-performance analog interface has a 65-dB S/(N+D) ADC and a 72-dB S/(N+D) DAC, which is useful in high-quality speech processing. Also included are programmable gain stages and on-chip anti-aliasing and anti-imaging filters.

Typical power dissipation with 5-volt supply is 400 mW at 26 MIPs. To conserve energy in battery-powered equipment, a <1-mW power-down mode is available with recovery within 100 clock cycles (7.7 µs, using the 13-MHz input clock required for 26 MIPs).

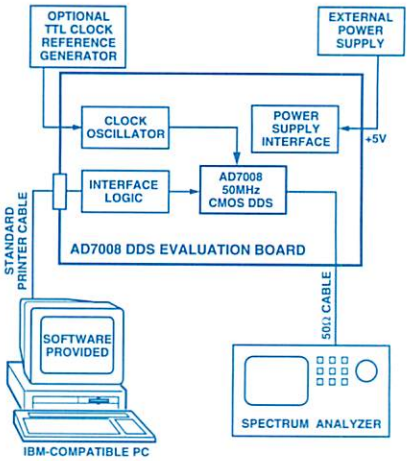
The ADSP-21msp58/59 mixed-signal processors are available in the extended industrial temperature grade (–40 to +85°C). Prices begin at $25 in 10,000s. **Circle 18**

Evaluation Board for DDS Waveforms

AD7008/PCB includes hardware & PC software Controls amplitude, frequency, phase to 25 MHz

The AD7008/PCB is a fully configured evaluation board for direct-digital-synthesis (DDS) implementations. It provides a simple, compact, time-saving, fully designed and tested solution for engineers who want to evaluate or use DDS systems in wireless applications. It includes all the hardware and software (running on any PC) to generate arbitrary waveforms (including quadrature), with complete control over amplitude, phase, and frequency for bandwidths of 25 MHz or less.

The board is based on the AD7008 (*Analog Dialogue* 27-2, p.24)—a complete single-chip DDS processor that integrates a numerically controlled oscillator with 32-bit phase accumulator, sine and cosine lookup tables, control circuitry, and a high-performance 10-bit DAC, to provide a precise analog output waveform. The digital design replaces expensive, hard-to-use complex multi-loop synthesizers that require significantly more board space; and the AD7008's 32-bit internal accuracy provides much better phase matching and stability than any analog approach. The AD7008/PCB is priced at $200. **Circle 19**



Microprocessor Supervisory Circuits

ADM705-708: monitors, reset, watchdog at low cost

The ADM705/706/707/708 constitute a family of low-cost µP supervisory circuits. (*Analog Dialogue* 28-1, p. 12). Their functions include power-on *reset* during power-ups, power-downs and brownout, a 1.25-V threshold detector for *power-fail warning*, detection of low-battery, or to monitor a supply other than 5 V, and an active-low debounced *manual reset* input. The ADM705/706 also have independent *watchdog timers* that go low if the watchdog input has not been toggled within 1.6 seconds. The ADM707/708 include an active-high reset.

Quiescent current is only 190 µA, and $\overline{\text{RESET}}$ is guaranteed with V_{CC}=1 V. The reset threshold is +4.65 V for ADM705/ 707 and 4.40 V for ADM706/708. All are available in 8-pin DIP& SO. Prices start at $0.84 (84¢) in 1000s. **Circle 20**

Voltage-monitoring for +3 and +3.3-V supplies

The ADM706P/R/S/T and the ADM708R/S/T perform similar functions to the ADM706 and ADM708, described in the adjacent column but are specifically intended for low-voltage processor applications. All of these types, in both columns, are superior upgrades for industry-standard devices having the same alphanumeric designations.

The various versions differ in that the P and R grades monitor 2.63-V threshold levels; the S monitors 2.93 V, and the T monitors 3.08 V. The ADM706P's reset output is active high, and all versions of the ADM708 have both active high and active low reset. Quiescent current for these devices is only 100 µA. All parts are available in 88-pin DIP and narrow SOIC packages. Prices start at $0.84 (84¢) in 1000s. **Circle 21**

Ask the Applications Engineer—17

MUST A "16-BIT" CONVERTER BE 16-BIT MONOTONIC AND SETTLE TO 16 PPM?

by Dave Robertson and Steve Ruscak

Q. *I recently saw a data sheet for a low-cost 16-bit, 30 MSPS D/A converter. On examination, its differential nonlinearity (DNL) was only at the 14 bit level, and it took 35 ns (1/28.6 MHz) to settle to 0.025% (12 bits) of a full scale step. Isn't this at best a 14 bit, 28 MHz converter? And if the converter is only 14-bit monotonic, the last two bits don't seem very effective; why bother to keep them? Can I be sure they're even connected?*

A. That's a lot of questions. Let's take them one at a time, starting with the last one. You can verify that the 15th and 16th bits are connected by exercising them and observing that 0..00, 0..01, 0..10, and 0..11 give a very nice 4-level output staircase, with each step of the order of 1/65,536 of full scale. You can see that they would be especially useful in following a waveform that spent some of its time swinging between 0..00 and 0..11, or providing important detail to one swinging through a somewhat wider range. This is the crux of the *resolution* spec, the ability of the DAC to output 2^{16} individual voltage levels in response to the 65,536 codes possible with a 16-bit digital word.

Systems that must handle both strong and weak signals require large dynamic range. A notable example of this is the DACs used in early CD player designs. These converters offered 16-20 bits of dynamic range but only about 14 bits of differential linearity. The somewhat inaccurate representation of the digital input was far less important than the fact that the dynamic range was much wider than that of LP records and allowed both loud and soft sounds to be reproduced with barely audible noise—and that the converters' low cost made CD players affordable.

The resolution is what makes a 16-bit DAC a "16-bit DAC". Resolution is closely associated with *dynamic range*, the ratio of the largest signal to the smallest *that can be resolved*. So dynamic range also depends on the noise level; the irreducible "noise" level in ideal ADCs or DACs is *quantization noise*.

Q. *What is quantization noise?*

A. The sawtooth-wave-shaped quantization noise of an ideal n-bit converter is the difference between a linearly increasing analog value and the stepwise-increasing digital value. It has an rms value of $1/(2^{n+1}\sqrt{3})$ of span, or $-(6.02\,n + 10.79)$ dB (below p-p full scale). For a sine wave, with peak-to-peak amplitude equal to the converter's span, rms is $\sqrt{2}/4$, or –9.03 dB, of span, so the full-scale signal-to-noise ratio of an ideal n-bit converter, expressed in dB, becomes the classical

$$6.02\,n + 1.76 \text{ dB}. \qquad (1)$$

As the analog signal varies through a number of quantization levels, the associated quantization noise resembles superimposed "white" noise. In a real converter, the circuit noise produced by the devices that constitute it adds to quantization noise in root-sum-of-squares fashion, to set a limit on the amplitude of the minimum detectable signal.

Q. *But I still worry about that differential nonlinearity spec. Doesn't 14-bit differential nonlinearity mean that the converter may be non-monotonic at the 16-bit level, i.e., that those last two bits have little influence on overall accuracy?*

A. That's true, but whether to worry about it depends on the application. If you have an instrumentation application that really requires 16-bit resolution, 1/2-LSB accuracy for all codes, and 1-LSB full-scale settling in 31.25 ns (we'll get to that discussion shortly), this isn't the right converter. But perhaps you really need 16-bit dynamic range to handle fine structure over small ranges, as in the above example, while high overall accuracy is not needed—and is actually a burden if cost is critical.

What you need to consider in regard to DNL in signal-processing applications is 1) the noise power generated by the DNL errors and 2) the types of signals that the D/A will be generating. Let's consider how these might affect performance.

In many cases, DNL errors occur only at specific places along the converter's transfer function. These errors appear as spurious components in the converter's output spectrum and degrade the signal-to-noise ratio. If the power in these spurs makes it impossible to distinguish the desired signal, the DNL errors are too large. Another way to think about it is as a ratio of the quantity of good codes to bad codes (those having large DNL errors). This is where the type of signal is important.

The various applications may concentrate in differing portions of the converter's transfer function. For example, assume that the D/A converter must be able to produce very large signals and very small signals. When the signals are large, there is a high proportion of DNL errors. But, in many applications, the signal-to-noise ratio will be acceptable because the signal is large.

Now consider the case where the signal is very small. The proportion of DNL errors that occur in the region of the transfer function exercised by the signal may be quite small. In fact, in this particular region, the spurs produced by the DNL errors could be at a level comparable to the converter's quantization noise. When the quantization noise becomes the limiting factor in determining signal-to-noise ratio, 16 bits of resolution will really make a difference (12 dB!) when compared to 14 bits.

Q. *OK, I understand. That's why there's such a variety of converters out there, and why I have to be careful to interpret the specs in terms of my application. In fact, maybe data sheets that have a great number of "typical" plots of parameters that are hard to spec are providing really useful information. Now, how about the settling-time question?*

A. *Update rate* for a D/A converter refers to the rate at which the digital input circuitry can accept new inputs, while *settling time* is the time the analog output requires to achieve a specified level of accuracy, usually with full-scale steps.

As with accuracy, time-domain performance requirements differ widely between applications. If full accuracy and full-scale steps are required between conversions, the settling requirements will be quite demanding (as in the case of offset correction with CCD image digitizers). On the other hand, waveform synthesis typically requires relatively small steps from sample to sample. The solid practical ground is that full-scale steps in consecutive samples mean operation at the Nyquist rate (half the sampling frequency), which makes it extremely difficult (how about "impossible"?) to design an effective anti-imaging filter.

Thus, DACs used for waveform reconstruction and many other applications* inevitably oversample. For such operation, full-scale settling is not required; and in general, smaller transitions require less time to settle to a given accuracy. Oversampled waveforms, taking advantage of this fact, achieve accuracy and speed greater than are implied by the full-scale specification.

*The AD768 is an example of such a DAC. Circle 22

Worth Reading

DATABOOK

DSP/MSP Products Reference Manual—1995. A 622-page databook on products for digital- and mixed-signal processing. Includes General information, Signal-processing products, Sound-processing products (computer audio), Sound-processing products (digital audio), Technical Support, Application notes. **Free, Circle 23**

SPICE LIBRARY

The latest update of our ADSPICE library on diskette, release K, contains 446 macromodels, including 6 new generics and 18 new models. New additions include the OP279, OP191, AD795, OP284, AD8001, and AD824. The library is complete on a file-compressed 1.44-Mbyte 3.5-inch diskette. **Free, Circle 24**

SERIAL PUBLICATIONS

DSPatch—The DSP Applications Newsletter: Number 32 (Winter, 1995) features the ADSP-2181. Also featured: Release 3.1 of software development tools for the floating-point ADSP-21xxx family, including SHARCs. Customer stories include Real Time Signal Processing's EZDSP-Lab, a high-performance data acquisition & processing system, a development system for the Macintosh, Brown University's LEMS microphone array system, a development board for the ISA bus, and various interesting DSP consulting projects from Canada. The C-programming series for DSP continues, plus regular features: Q&A, Up To Date, Workshop schedule, Current software releases, and Available literature. **Circle 25**

Analog Briefings, the newsletter for the defense/aerospace industry: **Number 10-1**, March, 1995, includes a cross-reference guide offer for functional replacements of Motorola's discontinued military ICs; DSP development tools and the SHARC processor; Quality systems, certifications, and product quality; various new products available to meet Standard Military Drawings (SMDs); etc. **Circle 26**

GUIDES

ADG508F Multiplexer Family Summary Guide: 6-page cross-reference to competitive products. **Free, Circle 27**

A Selection Guide for Serial DACs: 8-pages of serial 8-16-bit DACs for supplies from +3 to ±15 V. **Circle 28**

AUDIO PRODUCT HIGHLIGHTS. Circle 29

AD1812 SoundPort® Controller: 16-bit CD-quality sound on a chip. 2 pp.

LCPSS: Low Cost Personal Sound System multimedia-compatible audio reference design. 2 pp.

PSPro: Personal Sound Pro professional quality wavetable synthesis audio reference design. 2 pp.

PSCS IV: Personal Sound Comm System IV DSP audio/telephony reference design. 2 pp.

AD1845 SoundPort Stereo Codec product overview.

AD1843 Soundcomm Codec general product description.

ACCELEROMETER APPLICATION NOTES

Embedded shock and temperature recorder, by Bob Briano. [AN-383] **Circle 30**

Using accelerometers in low-*g* applications, by Charles Kitchin. [AN-374] **Circle 31**

Reducing the average power consumption of accelerometers, by Charles Kitchin, Mike Shuster, and Bob Briano. [AN-378] **Circle 32**

MORE AUTHORS *(continued from page 2)*

Charles Kitchin (page 10), is an Applications Engineer for the accelerometer product family. He has written more than 50 magazine articles and co-authored the *Rms-to-DC Conversion*-and *Instrumentation-Amplifier Application Guides*. Chuck has an ASET from Wentworth Institute and has studied E.E. at the University of Lowell. He enjoys wine tasting, amateur radio (call letters N1TEV), astronomy, and fishing.

Steve Martin (page 11) is a New Product Development Engineer for temperature sensors and automotive signal conditioning components in ADI's Transportation and Industrial Products division. He received BSEE and MSEE degrees from the University of Lowell. Steve has also worked in Applications. In his free time he enjoys skydiving, skiing, and reading about famous scientists.

Peter Checkovich (page 13), Applications Engineer for the Advanced Linear Products Division, supports analog signal processing ICs, op amps and video-encoder ICs. He has BSEE and MSEE degrees from Cornell. Prior to joining ADI, he worked in medical ultrasound, video recording, and optical detection for medical laser systems. In his spare time he enjoys carpentry and auto mechanics.

Steve Ruscak (page 21) is a Senior Applications Specialist in the High-Speed Converter group at Analog Devices in Wilmington, MA, specializing in communications- and imaging systems. He has a BSEE from Northeastern University. Before joining Analog Devices, he worked as a design engineer at Polaroid and General Electric. In his spare time, he enjoys cycling, woodworking, music, and his family.

Dave Robertson (page 21) is a design engineer in ADI's High-Speed Converter group in Wilmington, MA. He joined Analog on graduating from Dartmouth College, with BA and BE degrees. He has worked on high-speed D/A and A/D converters, including the AD568, AD668, AD773, AD872 and AD1871, and is now developing and adapting high-speed converters for communications systems. In his free time Dave plays rugby and entertains his two children.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

STOP PRESS—NEW PRODUCTS
Low-power 500-MHz mixer/log-limiter/80-dB RSSI—3-V receiver IF subsystem: **AD608. Circle 34**

Serial 16-bit high-performance voltage-output multiplying DAC with output clamped during on-off cycling: **AD7849. Circle 35**

DATA SHEETS, ERRATA • • • The AD7008 direct digital synthesis chip has a new data sheet (Rev. B). **Circle 36 • • •** A **new data sheet is available for the ADG508F/509F/528F** series of analog multiplexers (Rev. A). It explains more clearly about fault and overvoltage protection. **Circle 37 • • •** There's an **errata sheet for the AD608**. If you have the Rev. 0 data sheet, but no errata information, **Circle 38**

IN THE LAST ISSUE

Volume 28, Number 3, 1994, 24 Pages
For a copy, circle 33.

Editor's Notes
Floating-point DSP leads in memory, interconnectivity, performance (SHARC)
Fast, low-distortion V-feedback op amps with clamping (AD9631/2,AD8036/7)
New high-speed A/D converters for communications (AD9022/23/26/27)
New 8-bit, 16-channel voltage-output D/A converter (AD8600)
16-bit DAC for comms, imaging & displays updates @ 30 MHz (AD768)
12-bit dual DAC: Serial, single-supply, saves space in SO-14 (AD8522)
16-bit fixed point DSP: 80 Kbytes of RAM reduce system cost (ADSP-2181)
Simple techniques protect amplifiers from high-voltage inputs
New-Product Briefs:
What's new in amplifiers: VCAs, transimpedance, isolation, µpower
What's new in interfaces: RS-232, RGB-to-NTSC/PAL
What's new in A/D and D/A converters
What's new in switches, voltage references, motion control
What's new in digital audio: ASRC, personal sound, codec
Worth Reading
Potpourri

PRODUCT NOTES • • • Evaluation boards are available —at reasonable prices—for many new Analog Devices ICs. They will help you with the speedy evaluation and design-in of a product **• • • Rev. 3.1 software is available for ADI floating-point processors—including SHARCs • • •** The **integral nonlinearity spec for B-grade AD7884 and AD7885 is now 0.0075% FSR max**. A grade and all other specs are unchanged **• • • Because an accelerometer needs attention to both electrical and mechanical installation considerations, designers may be inhibited** from going into the details of applying an ADXL type, **especially for multiple-axis applications**. If this is true in your case, you may be interested to know about a rapidly burgeoning applications-oriented breed known as **"accelerometer repackagers", who have solved the problem you don't want to reinvent. They can provide 1-, 2-, and 3-axis** acceleration-measuring packages. Two such companies in the U.S. that have come to our attention are **NGT Technologies**, LaGrangeville NY [**(914) 223-3359**] and **Summit Instruments**, Akron, Ohio [**(216) 659-3312**]. Consult our accelerometer application engineers for more names **• • •** A new, **highest-accuracy, monolithic resolver-to-digital converter, the AD2S80AWD**, is now available, as a **1.3-arc-minute grade** of the popular AD2S80. Consult the sales force for further information **• • •** The **AD420 serial 16-bit current-loop industrial DAC** has a new **32-volt version at a saving in price over the standard 36-V version**. For information, ask about the AD420AR-32 and AD420AN-32.

SEMINARS AND SHOWS • • • Shows we will be exhibiting at in the near future include DSPx '95, **May 16-18 in San Jose CA**; Sensors Expo '95, **May 16-18, in Boston MA**; PCIM '95, **June 20-22, in Nürnberg, Germany**; Sensors Expo '95, **September 12-14, Rosemont, IL**; AES (Audio Engineering Show) '95, **October 5-8, New York City**; Japan Electronics Show '95, **October 17-21, Osaka, Japan**; DSPWorld '95, **October 24-26, Boston MA**; and Comdex/Fall '95, **November 13-17, Las Vegas NV**. If you're in the neighborhood, drop in and see us **• • •** The Analog Devices **1995 domestic Design Seminar series—"Practical Analog Design Techniques"** is in full swing. Remaining seminars as of our publication date will take place in Orlando and Fort Lauderdale **FL**, Atlanta **GA**, Dedham **MA**, Nashua **NH**, Rochester **NY**, Cleveland **OH**, Portland **OR**, Harrisburg **PA**, and Austin **TX**. Call **1-800-262-5643 or (617) 937-1430 for information and to reserve your place.**

PATENTS • • • 5,313,205 to James Wilson for **Method for varying the interpolation ratio of a digital oversampling D/A converter system and apparatus therefor • • •** 5,362,681 to Carl M. Roberts, Jr., Lewis H. Long, and Paul A. Ruggerio for **Method for separating circuit dies from a wafer • • •** 5,364,497 to Kevin H. L. Chau, Michael P. Saltmarsh, and Deborah A. Church for **Method for fabricating microstructures using temporary bridges • • •** 5,373,400 to Janos Kovacs for **Dynamic threshold updating circuit for a maximum likelihood detector using both positive and negative comparators • • •** 5,375,228 to Kevin W. Leary and Russell L. Rivin for **Real-time signal analysis apparatus and method for digital signal processor emulation • • •** 5,381,148 to Michael Mueck and Paul F. Ferguson, Jr., for **Method and apparatus for calibrating a gain control circuit • • •** 5,387,912 to Derek F. Bowers for **Digital-to-analog converter with reference glitch reduction • • •** 5,387,914 to Christopher W. Mangelsdorf for **Correction range technique for multirange converter • • •** 5,389,811 to Frank Poucher and John Quill for **Fault-protected overvoltage switch employing isolated transistor tubs • • •** 5,394,019 to Jonathan M. Audy for **Electrically trimmable resistor ladder • • •** 5,398,048 to Denis O'Mahony for **Integrated-circuit chip and system for developing timing reference signals for use in high-resolution CRT display equipment**.

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